



# SERVICE MANUAL

VHF MOBLE TRANSCEIVERS

**IC-F1721/D**  
**IC-F1710**  
**IC-F1821/D**  
**IC-F1810**

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## INTRODUCTION

This service manual describes the latest service information for the **IC-F1721/D/F1710/F1821/D/F1810** VHF MOBILE TRANSCEIVER at the time of publication.

6 versions of the **IC-F1721** have been designed. This service manual covers each version.

MODEL	VERSION	10 KEY	TX power
IC-F1721D	USA-02, USA-03	None	50 W
IC-F1721	USA-04		25 W
IC-F1710	EUR-02, GEN-02		
IC-F1821D	USA-02, USA-03	Yes	50 W
IC-F1821	USA-04		25 W
IC-F1810	EUR-02, GEN-02		

To upgrade quality, any electrical or mechanical parts and internal circuits are subject to change without notice or obligation.

## DANGER

**NEVER** connect the transceiver to an AC outlet or to a DC power supply that uses more than 16 V. This will ruin the transceiver.

**DO NOT** expose the transceiver to rain, snow or any liquids.

**DO NOT** reverse the polarities of the power supply when connecting the transceiver.

**DO NOT** apply an RF signal of more than 20 dBm (100mW) to the antenna connector. This could damage the transceiver's front end.

**IC-F1700 Series**



**IC-F1e00 Series**



## ORDERING PARTS

Be sure to include the following four points when ordering replacement parts:

1. 10-digit order numbers
2. Component part number and name
3. Equipment model name and unit name
4. Quantity required

### <SAMPLE ORDER>

1110003490 S.I.C TA31136FN IC-F1721 MAIN UNIT 5 pieces  
8820001210 Screw 2438 screw IC-F1721 Chassis 12 pieces

Addresses are provided on the inside back cover for your convenience.

## REPAIR NOTES

1. Make sure a problem is internal before disassembling the transceiver.
2. **DO NOT** open the transceiver until the transceiver is disconnected from its power source.
3. **DO NOT** force any of the variable components. Turn them slowly and smoothly.
4. **DO NOT** short any circuits or electronic parts. An insulated turning tool **MUST** be used for all adjustments.
5. **DO NOT** keep power ON for a long time when the transceiver is defective.
6. **DO NOT** transmit power into a signal generator or a sweep generator.
7. **ALWAYS** connect a 40 dB to 50 dB attenuator between the transceiver and a deviation meter or spectrum analyzer when using such test equipment.
8. **READ** the instructions of test equipment thoroughly before connecting equipment to the transceiver.

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# SECTION 1 SPECIFICATIONS

## ■ GENERAL

- Frequency coverage
- Type of emission

: 136.000–174.000 MHz

VERSION	WIDE	MIDDLE	NARROW
[USA]			11K0F3E (12.5 kHz)
[GEN]	16K0F3E (25.0 kHz)	N/A	
[EUR]		14K0F3E (20.0 kHz)	8K50F3E (12.5 kHz)

- Number of conventional channels
- Antenna impedance
- Operating temperature range
- Power supply requirement  
(Negative ground)
- Current drain (Approx.)

: max 256 channels

: 50 Ω

: –30°C to +60°C (–22°F to +140°F)

: 13.6 V DC nominal

: 13.2 V DC nominal

[USA], [GEN]

[EUR]

RECEIVING		TRANSMITTING	
Stand-by	Max. audio	at 50 W	at 25 W
600 mA	1200 mA	14.0 A	7.0 A

- Dimensions (projections not included)
- Weight (Approx.)

: 175(W) × 45(H) × 170(D) mm; 6<sup>7</sup>/<sub>8</sub>(W) × 1<sup>25</sup>/<sub>32</sub>(H) × 6<sup>11</sup>/<sub>16</sub>(D) in

: 1.5 kg; 3<sup>5</sup>/<sub>16</sub> lb

## ■ TRANSMITTER

- Output power
- Modulation
- Maximum permissible deviation
- Frequency error
- Spurious emissions
- Adjacent channel power
- Audio harmonic distortion
- Limiting charact of modulator
- Microphone impedance

: 25 W	[F1710], [F1810]
: 50 W	[F1721/D], [F1821/D]
: Variable reactance frequency modulation	
: ±5.0 kHz (Wide), ±4.0 kHz (Middle), ±2.5 kHz (Narrow)	
: ±2.0 ppm	[USA], [GEN]
: ±0.85 kHz	[EUR]
: 75 dB (typical)	[USA], [GEN]
: 0.25 μW ( $\leq$ 1 GHz), 1.0 μW ( $>$ 1 GHz)	[EUR]
: 70 dB min. for Wide and Middle	
: 60 dB min. for Narrow	
: 3% typical (Mod. 1 kHz, 40% deviation)	
: 70–100% of maximum deviation	
: 600 Ω	

## ■ RECEIVER

- Receive system
- Intermediate frequencies
- Sensitivity
- Adjacent channel selectivity
- Spurious response
- Intermodulation rejection ratio
- Audio output power  
(Internal)  
(External)
- Squelch sensitivity (at threshold)
- Output impedance (Audio)

: Double conversion superheterodyne system	
: 1st IF: 46.35 MHz, 2nd IF: 450 kHz	
: 0.25 μV ( $-119$ dBm) typical at 12 dB SINAD	[USA], [GEN]
: –4 dB $\mu$ V emf typical at 20 dB SINAD	[EUR]
: 70 dB min. (80 dB typical) for Wide and Middle	
: 60 dB min. (75 dB typical) for Narrow	
: 70 dB min. (80 dB typical)	
: 70 dB min. (77 dB typical) for Wide	[USA], [GEN]
: 70 dB min. (75 dB typical) for Narrow	[USA], [GEN]
: 65 dB min. (70 dB typical)	[EUR]
: 4 W typical at 10% distortion with a 4 Ω load	
: 22 W typical (BTL) at 10% with a 4 Ω load (D-SUB 25 connector)	
: 0.25 μV typical	[USA], [GEN]
: –4 dB $\mu$ V emf typical	[EUR]
: 4 Ω	

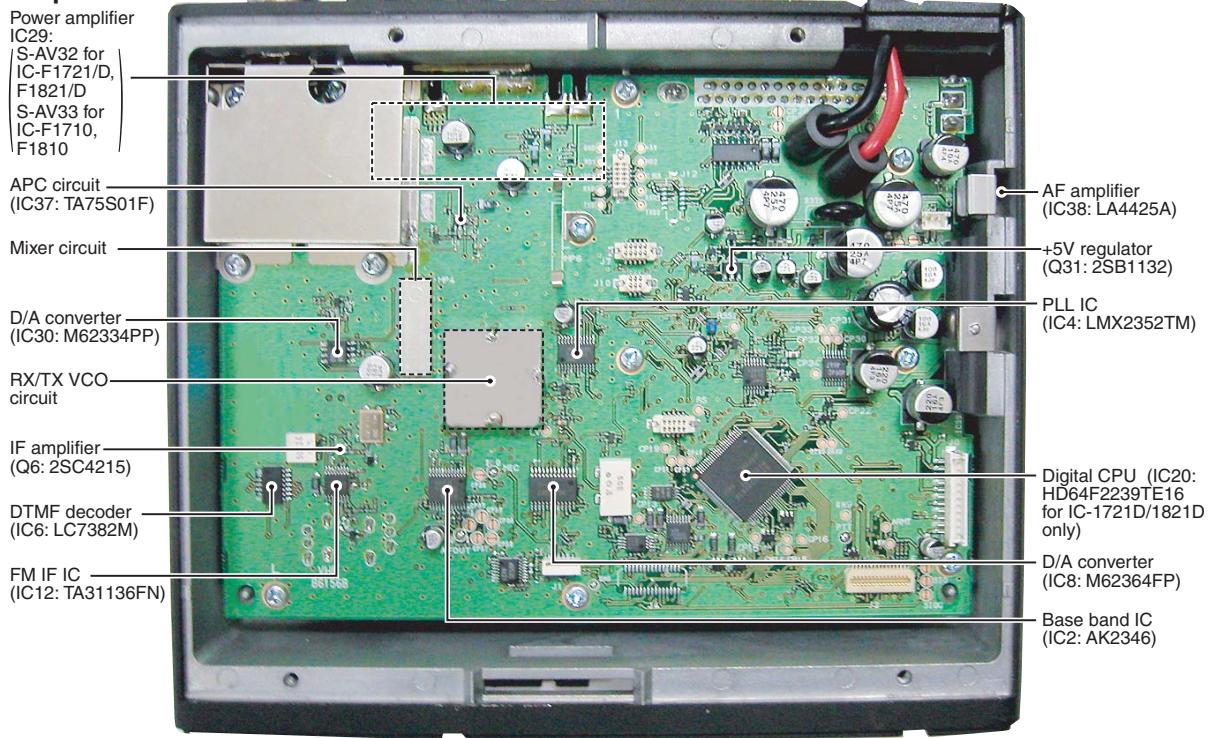
Specifications are measured in accordance with EIA-152-C/204D, TIA-603 or EN 300 086.

All stated specifications are subject to change without notice or obligation.

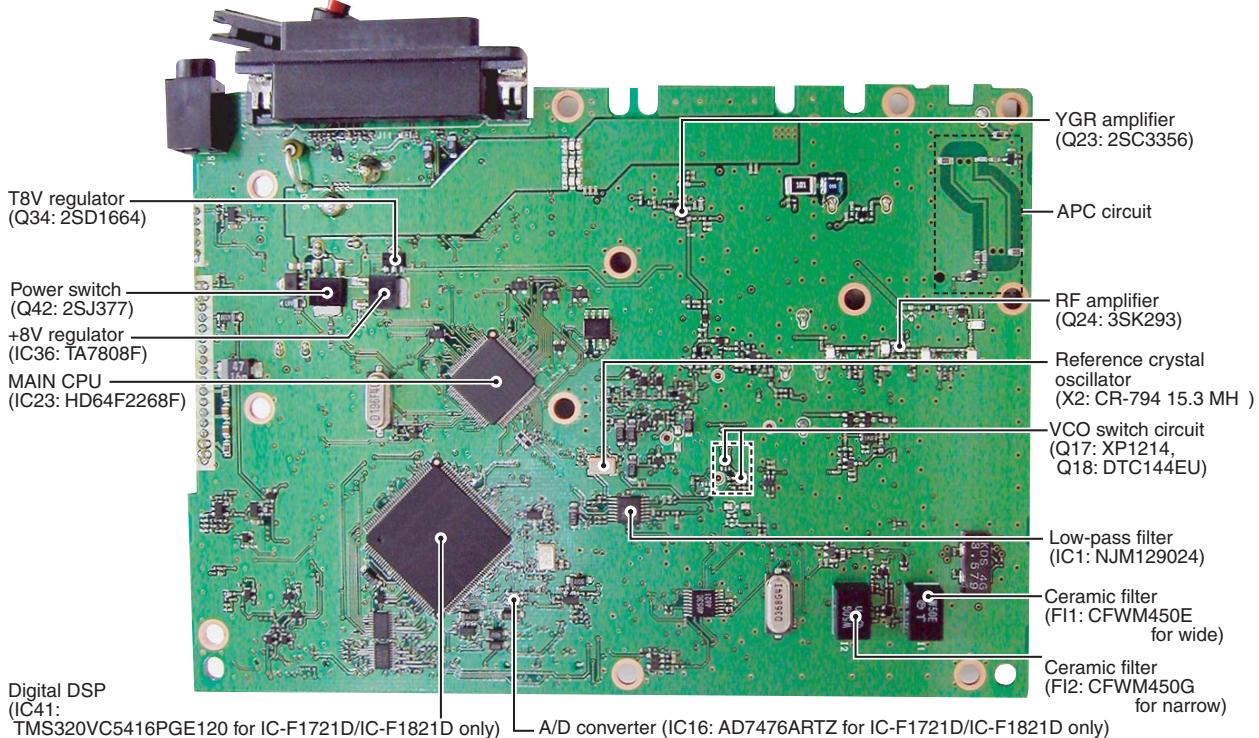
## SECTION 2 INSIDE VIEWS

### • MAIN UNIT

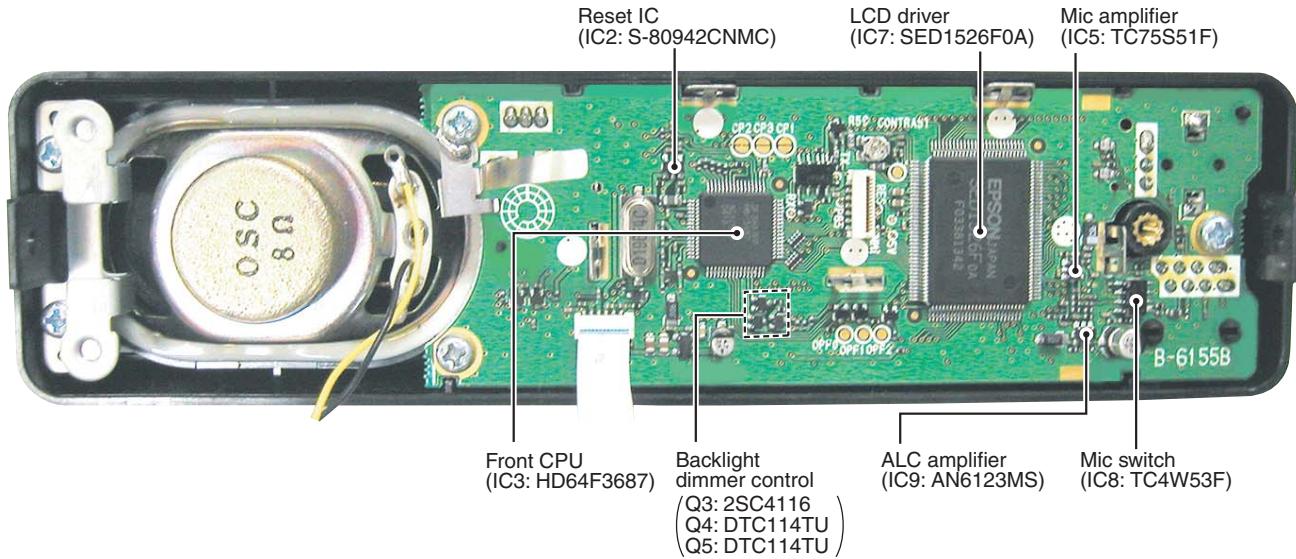
#### Top view



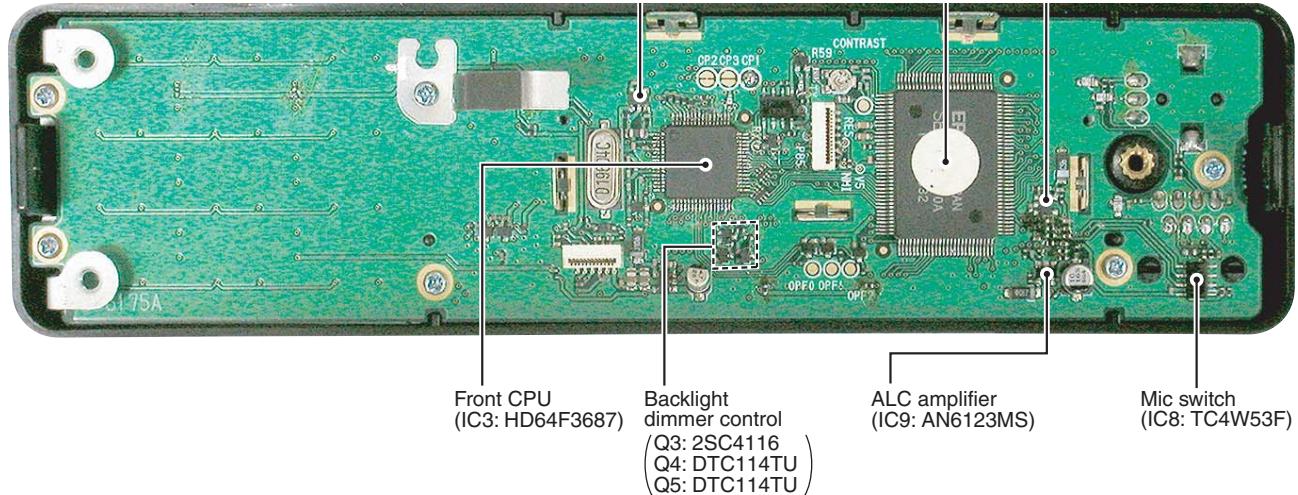
#### • Bottom view



• FRONT-A UNIT (IC-F1700 Series)



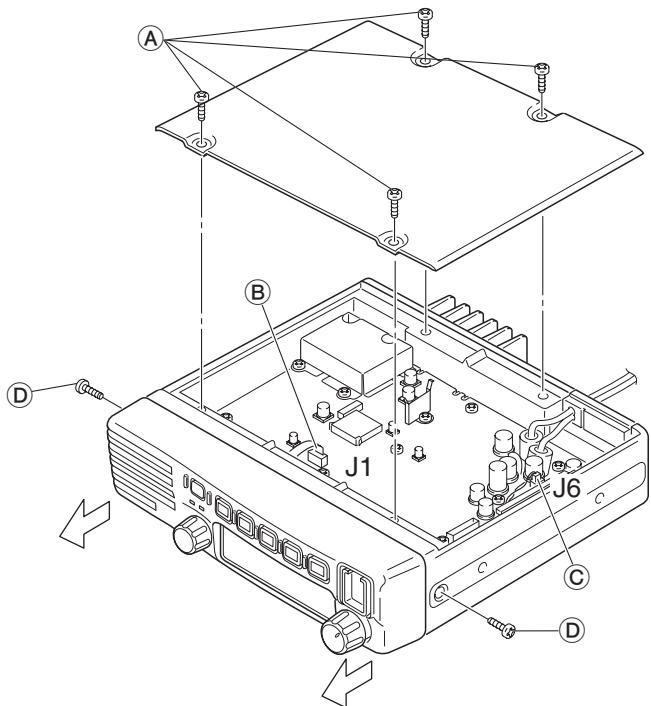
• FRONT-B UNIT (IC-F1800 Series)



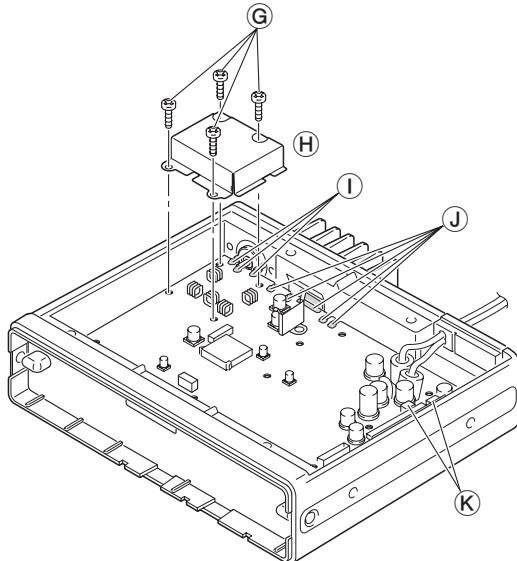
## SECTION 3 DISASSEMBLY INSTRUCTIONS

### • REMOVING THE FRONT UNIT

- ① Unscrew 4 screws, A, then remove the bottom cover.
- ② Unplug J1(B) and J6 (C).
- ③ Unscrew 2 screws, D.
- ④ Remove the front unit in the direction of the arrow.



- ② Unscrew 4 screws, G and remove the shield cover H.
- ③ Unsolder 3 points, I and 5 points J.
- ④ Remove 2 clips, K.

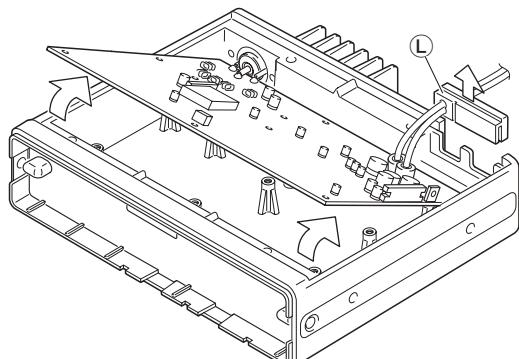
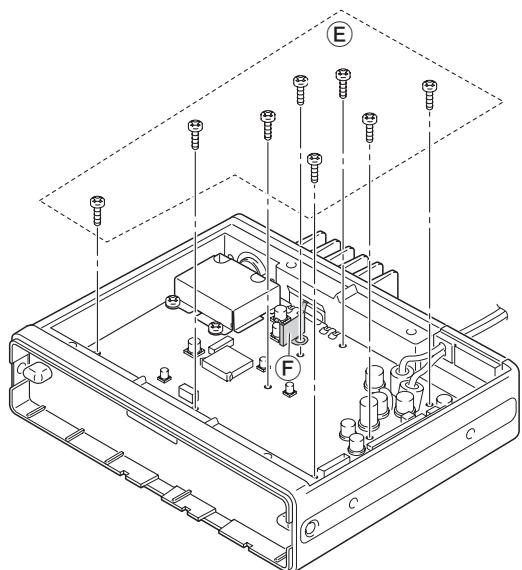


### • REMOVING THE MAIN UNIT

- ① Remove the bushing, L.
- ② Remove the MAIN unit in the direction of the arrow.

### • BEFORE REMOVING THE MAIN UNIT

- ① Unscrew 8 screws, E and remove the shield plate F.



Continue to right above

## SECTION 4 CIRCUIT DESCRIPTION

### 4-1 RECEIVER CIRCUITS

#### 4-1-1 ANTENNA SWITCHING CIRCUIT (MAIN UNIT)

The antenna switching circuit functions as a low-pass filter while receiving and a resonator circuit while transmitting. This circuit does not allow transmit signals to enter the receiver circuits.

Received signals enter the antenna connector (CHASSIS; J1) and pass through the low-pass filters (L42–L44, C375, C388, C389, C391, C432, C461). The filtered signals are passed through the  $\frac{1}{4}$  type antenna switching circuit (D29, D30) and then applied to the RF circuit.

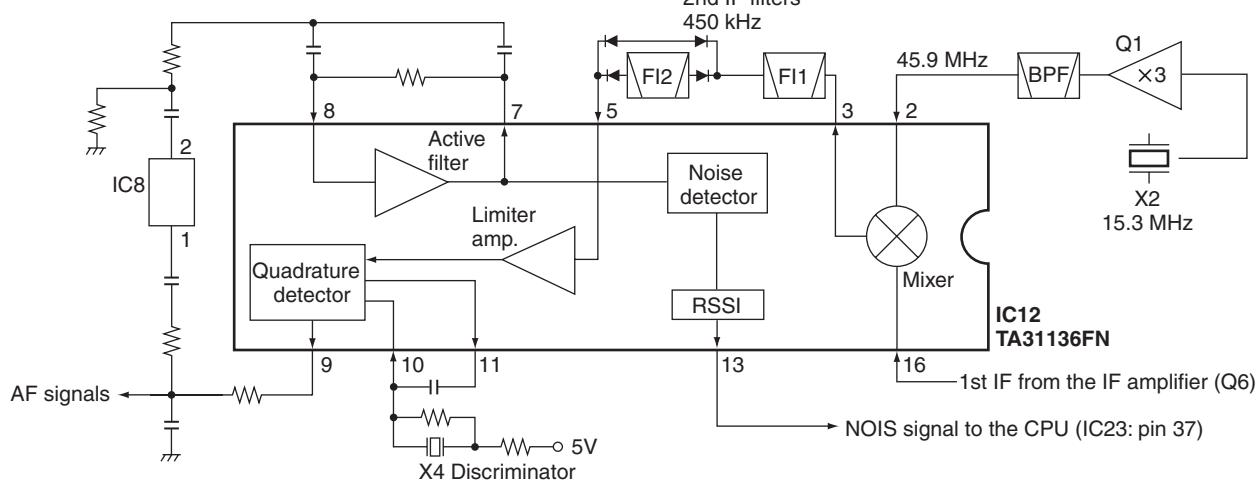
#### 4-1-2 RF CIRCUIT (MAIN UNIT)

The RF circuit amplifies signals within the range of frequency coverage and filters out-of-band signals.

The signals from the antenna switching circuit pass through the two-stage tunable bandpass filters (D23, D26, L32, L36). The filtered signals are amplified at the RF amplifier (Q24) and then passed through the another two-stage tunable bandpass filters (D17, D18, L28) to suppress unwanted signals. The filtered signals are applied to the 1st mixer circuit.

D17, D18, D23 and D26 employ varactor diodes, that are controlled by the MAIN CPU (IC23) via the D/A converter (IC30, pins 1, 2), to track the bandpass filter. These varactor diodes tune the center frequency of an RF passband for wide bandwidth receiving and good image response rejection.

#### • 2ND IF AND DEMODULATOR CIRCUITS



#### 4-1-3 1ST MIXER AND 1ST IF CIRCUITS (MAIN UNIT)

The 1st mixer circuit converts the received signals into fixed frequency of the 1st IF signal with the PLL output frequency. By changing the PLL frequency, only the desired frequency passes through a monolithic filter at the next stage of the 1st mixer.

The RF signals from the bandpass filter are mixed with the 1st LO signals, where come from the RX VCO circuit (Q11, D6, D7) via the LO amplifier (Q21) and low-pass filter (L24, C246, C264), at the 1st mixer circuit (D16, L22, L23) to produce a 46.35 MHz 1st IF signal. The 1st IF signal is passed through a monolithic filter (F14) to supplies unwanted signals and to pass only the desired signals after being amplified at the IF amplifiers (Q10, Q13, Q14). The filtered signal is applied to the 1st IF amplifier (Q6) and then applied to the 2nd IF circuit.

#### 4-1-4 2ND IF AND DEMODULATOR CIRCUITS (MAIN UNIT)

The 2nd mixer circuit converts the 1st IF signal into a 2nd IF signal. The double-conversion superheterodyne system (which convert receive signals twice) improves the image rejection ratio and obtains stable receiver gain.

The 1st IF signal from the IF amplifier (Q6) is applied to the 2nd mixer section of the FM IF IC (IC12, pin 16), and is mixed with the 2nd LO signal to be converted into a 450 kHz 2nd IF signal.

The FM IF IC (IC12) contains the 2nd mixer, limiter amplifier, quadrature detector, active filter and noise amplifier circuits.

A 2nd LO signal (45.9 MHz) is produced at the PLL circuit by tripling its reference frequency (15.3 MHz).

The 2nd IF signal from the 2nd mixer section (IC12, pin 3) passes through the ceramic filter(s) (Wide: FI1 only, Narrow: FI1 and FI2) to remove unwanted heterodyned frequencies. It is then amplified at the limiter amplifier section (IC12, pin 5) and applied to the quadrature detector section (IC12, pins 10, 11) to demodulate the 2nd IF signal into AF signals.

The demodulated AF signals are output from pin 9 (IC12) and applied to the base band IC (IC2).

#### 4-1-5 AF AMPLIFIER CIRCUIT (MAIN UNIT)

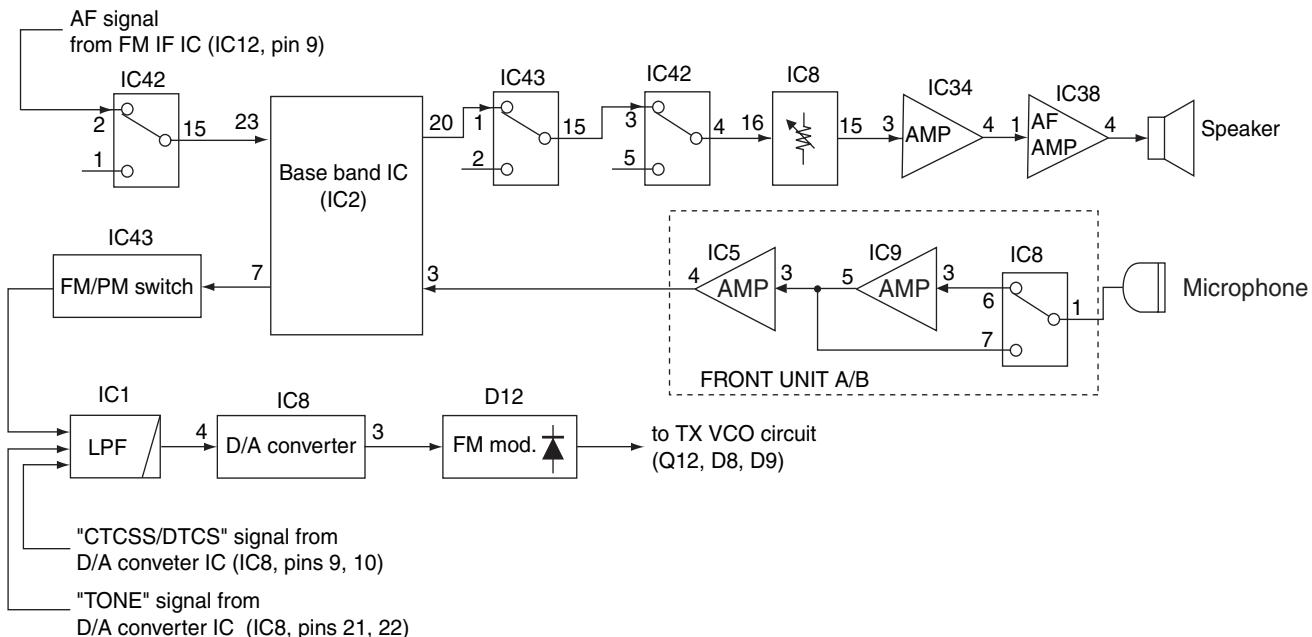
The AF amplifier circuit amplifies the demodulated AF signals to drive a speaker. This transceiver employs the base band IC which is composed of pre-amplifier, expander, scrambler, MSK de-modulator, etc. at the AF amplifier section.

The AF signals from the FM IF IC (IC12, pin 9) are passed through the DA switch (IC42, pins 2, 15) and are then applied to the base band IC (IC2, pin, 23). The signals are amplified at the AF amplifier section in the base band IC (IC2, pin 23), and are then applied to the high-pass and low-pass filter sections of it.

The filtered signals pass through the high-pass filter to suppress unwanted harmonic components. The signals pass through (or bypass) scrambler and expander sections. The signals are amplified at the amplifier section in the base band IC (IC2).

The output signals from the base band IC (IC2, pin 20) are applied to the AF volume (IC8, pins 15, 16), and are then applied to the AF power amplifiers (IC34 pins 3, 4, IC38 pins 1, 4) after pass through the analog switches (IC42 pins 3, 4 and IC43 pins 1, 15).

#### • AF AND MIC AMPLIFIER CIRCUITS



The power amplified AF signals are applied to the internal speaker (IC-F1700 series only) that is connected to J6 via [EXT SP] jack (J5).

#### 4-1-6 SQUELCH CIRCUITS (MAIN UNIT)

##### • NOISE SQUELCH

A squelch circuit cuts out AF signals when no RF signals are received. By detecting noise components in the AF signals, the squelch circuit switches the AF amplifier controller.

Some noise components in the AF signals from the FM IF IC (IC12, pin 9) are passed through the D/A converter (IC8, pins 1, 2). The signals are applied to the active filter section in the FM IF IC (IC12, pin 8). The active filter section filters and amplifies noise components. The amplified signals are converted into the pulse-type signals at the noise detector section. The detected signals output from pin 13 (NOIS) via the noise comparator section.

The "NOIS" signal from the FM IF IC is applied to the MAIN CPU (IC23, pin 37). Then the MAIN CPU analyzes the noise condition and outputs the AF mute signal as "AFON" from the pin 19 to the AF power controller (Q28, Q29, D34, D36).

##### • CTCSS AND DTCS

The tone squelch circuit detects tone signals and opens the squelch only when receiving a signal containing a matching subaudible tone (CTCSS or DTCS). When tone squelch is in use, and a signal with a mismatched or no subaudible tone is received, the tone squelch circuit mutes the AF signals even when noise squelch is open.

A portion of the AF signals from the FM IF IC (IC12, pin 9) pass through the low-pass filter (IC1, pins 8, 10) to remove AF (voice) signals, and are then applied to the amplifier (IC1, pins 5, 7). The amplified signals are applied to the CTCSS or DTCS decoder in the MAIN CPU (IC23, pin 46) via the "CDEC" line. The MAIN CPU outputs the AF mute signal as "AFON" from the pin 19 to the AF power controller (Q28, Q29, D34, D36).

## 4-2 TRANSMITTER CIRCUITS

### 4-2-1 MICROPHONE AMPLIFIER CIRCUIT (MAIN UNIT)

The microphone amplifier circuit amplifies audio signals within +6 dB/octave pre-emphasis 6characteristics from the microphone to a level needed for the modulation circuit.

This transceiver employs the base band IC which is composed of microphone amplifier, compressor, scrambler, limiter, splatter filter, MSK modulator, etc. at the microphone amplifier section.

The AF signals from the microphone connector (FRONT UNIT; J2, pin 6) are passed through the microphone switch (FRONT UNIT; IC8, pins 1, 6, 7) and are then applied to the ALC amplifier (FRONT UNIT; IC9) during digital mode operation (bypass during FM mode operation). The signals are amplified at the microphone amplifier (FRONT UNIT; IC5, pins 3, 4) and then applied to MAIN UNIT via J1 (pin 10).

The amplified signals are applied to the microphone amplifier section of the base band IC (IC2, pin 3). The amplified signals are passed through (or bypass) the compressor, scrambler sections of IC2, and are then passed through the high-pass, limiter amplifier, splatter filter sections of IC2.

The output signals from the base band IC (IC2, pin 7) are applied to the FM/PM switch (IC43, pins 12–14) after pass through the DA switch (IC42, pins 12, 14). The signal are passed through the low-pass filter (IC1, pins 4, 13) and then applied to the D/A converter (IC8, pins 3, 4). The output signal from D/A converter (IC8, pin 3) are applied to the modulation circuit (D12).

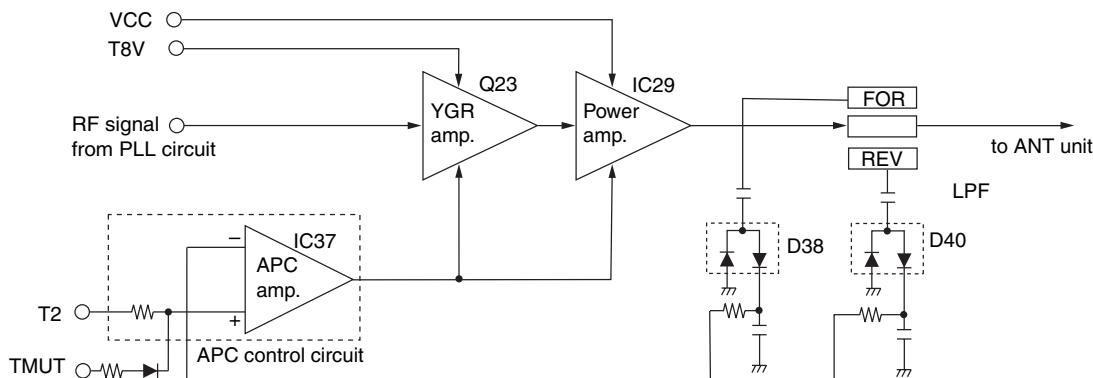
### 4-2-2 MODULATION CIRCUIT (MAIN UNIT)

The modulation circuit modulates the VCO oscillating signal (RF signal) using the microphone audio signals.

The AF signals from the D/A converter (IC8, pin 3) change the reactance of varactor diode (D12) to modulate the oscillated signal at the TX VCO circuit (Q12, D8, D9). The modulated VCO signal is amplified at the buffer amplifiers (Q20, Q22) and is then applied to the YGR amplifier circuit via the T/R switch (D19).

The CTCSS/DTCS signals ("CENC0", "CENC1", "CENC2") from the MAIN CPU (IC23, pins 89–91) are combined at resistors (R158, R159, R162) and are then pass through the low-pass filter (IC9, pins 8, 10).

#### • APC CIRCUIT



The filtered signals are applied to the D/A converter (IC8, pins 9, 10), and are then mixed with the filtered microphone audio signals. The mixed signals are applied to the D/A converter (IC8, pin 3, 4) after pass through the low-pass filter (IC1, pins 4, 13). The output signal from D/A converter (IC8, pin 3) are applied to the D12 in the TX VCO circuit.

### 4-2-3 YGR/POWER AMPLIFIER CIRCUITS (MAIN UNIT)

The YGR/power amplifier circuits amplify the VCO oscillating signal to an output power level.

The signal from the VCO circuit passes through the T/R switch (D19), and is amplified at the YGR (Q23), power (IC29) amplifiers to obtain 50 W (IC-F1721/D/F1821/D; 25 W for IC-F1710/F1810) of RF power.

The amplified signal is passed through the low-pass filter (L35, C345, C346, C348, C349), antenna switching circuit (D29, D30), low-pass filters (L42, L43, C375, C388, C389, C391), power detector (D38, D40), low-pass filter (L44, C432, C461), and is then applied to the antenna connector (CHASSIS unit; J1).

The bias voltage of the YGR amplifier (Q23) and power amplifier (IC29) are controlled by the APC circuit.

### 4-2-4 APC CIRCUIT (MAIN UNIT)

The APC circuit protects the power amplifier from a mismatched output load and stabilizes the output power.

The power detector circuit (D38, D40) detects the forward signals and reflection signals and converts it into DC voltage. The output voltage is at a minimum level when the antenna impedance is matched with 50 Ω and is increased when it is mismatched.

The detected voltage is applied to the differential amplifier (IC37; pins 3, 4), and the "T2" signal from the D/A converter (IC30, pin 2), controlled by the MAIN CPU (IC23), is applied to the other input for reference (IC37, pin 1). When antenna impedance is mismatched, the detected voltage exceeds the power setting voltage. Then the output voltage of the differential amplifier (IC37, pin 4) controls the bias voltage of the YGR amplifier (Q23) and power amplifier (IC29) amplifiers to reduce the output power.

## 4-3 PLL CIRCUITS

### 4-3-1 PLL CIRCUIT (MAIN UNIT)

A PLL circuit provides stable oscillation of the transmit frequency and receive 1st LO frequency. The PLL output compares the phase of the divided VCO frequency to the reference frequency. The PLL output frequency is controlled by the divided ratio (N-data) of a programmable divider.

The PLL circuit contains the RX VCO (Q11, D6, D7) and TX VCO (Q12, D8, D9). The oscillated signal is amplified at the buffer amplifier (Q20). The output signal frequency is doubled at Q19, and is then applied to the PLL IC (IC4, pin 6) after being passed through the bandpass filter (Q5, D3, D5, L4, L47, L48, C85, C104, C105, C123, C519–521).

Q5, D3 and D5 switch the filtering frequencies between TX and RX which is controlled by TXC.

The PLL IC contains a prescaler, programmable counter, programmable divider and phase detector, etc. The applied signal is divided at the prescaler and programmable counter section by the N-data ratio from the MAIN CPU. The divided signal is detected on phase at the phase detector using the reference frequency and output from pin 4. The output signal is passed through the loop filter (Q46, Q47) and is then applied to the VCO circuit.

If the oscillated signal drifts, its phase changes from that of the reference frequency, causing a lock voltage change to compensate for the drift in the oscillated frequency.

### 4-3-2 VCO CIRCUITS (MAIN UNIT)

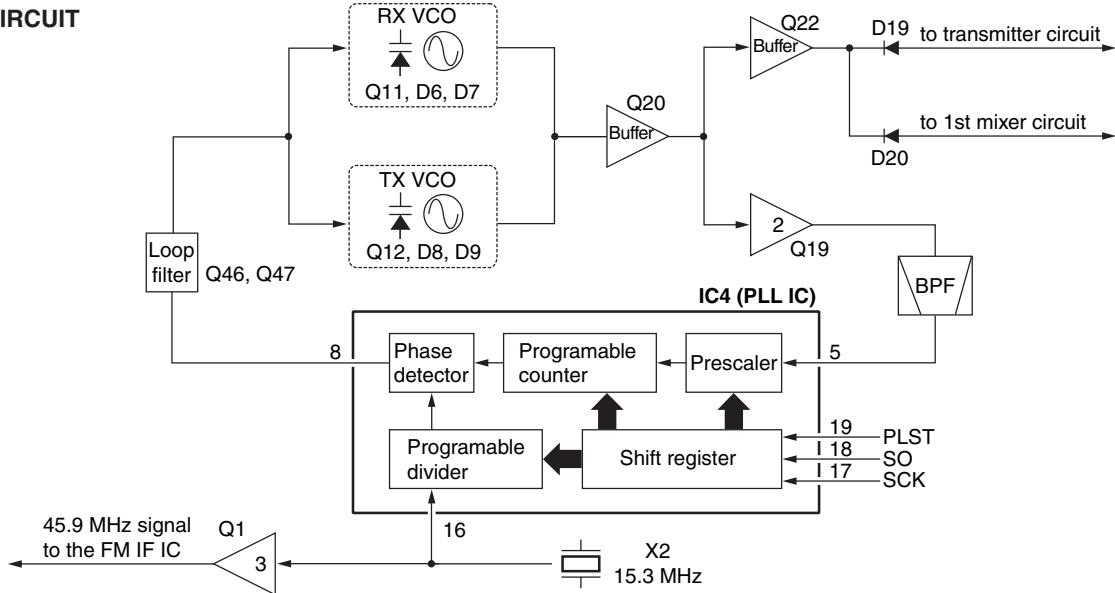
The VCO circuits contains a separate RX VCO (Q11, D6, D7) and TX VCO (Q12, D8, D9). The oscillated signal is amplified at the buffer amplifiers (Q20, Q22) and is then applied to the T/R switch (D19, D20). Then the receive 1st LO (Rx) signal is applied to the 1st mixer (L22, L23, D16) and the transmit (Tx) signal to the YGR amplifier circuit (Q23).

A portion of the signal from the buffer amplifier (Q20) is fed back to the PLL IC (IC4, pin 6) via the doubler circuit (Q19) as the comparison signal.

## 4-4 POWER SUPPLY CIRCUITS

Line	Description
HV	The voltage from a DC power supply.
VCC	The same voltage as the HV line which is controlled by the power switch circuit (Q41, Q42). When the [ ] is pushed, the MAIN CPU outputs the "PWR" control signal to the power switch circuit to turn the circuit ON.
CPU 5	Common 5 V converted from the HV line at the CPU5V regulator circuit (IC40). The output voltage is applied to the MAIN CPU (IC23) and EEPROM (IC26), etc.
5V	Common 5 V converted from the CPU5V line at the 5 V regulator circuit (Q31, Q32). The output voltage is applied to the PLL IC (IC4) and D/A converter IC (IC30), etc.
8V	Common 8 V converted from the VCC line at the 8 V regulator circuit (IC36). The output voltage is applied to the buffer amplifier (Q22) and 1st LO amplifier (Q21), etc.
T8V	Transmit 8 V controlled by the T8V regulator circuit (Q34) using the "TMUT" signal from the MAIN CPU (IC23). The output voltage is applied to the driver (Q23) and PA amplifiers (IC29), etc.
R8V	Receive 8 V controlled by the R8V regulator circuit (Q30) using the "TXC" signal from the MAIN CPU (IC23). The output voltage is applied to the RF amplifier (Q24) and 1st IF amplifier (Q6), etc.

### • PLL CIRCUIT



## 4-5 OTHER CIRCUITS

### 4-5-1 COMPANDER CIRCUIT (MAIN UNIT)

IC-F1700/F1800 series have compander circuit which can improve S/N ratio and become wide dynamic range. The circuit is composed in the base band IC (IC2).

#### (1) IN CASE OF RECEIVING

The demodulated AF signals from the FM IF IC (IC12, pin 9) are applied to the amplifier section in base band IC (IC2, pin 23), and then pass through the low-pass and high-pass filter section to suppress unwanted signals. The filtered signals pass through (or bypass) scrambler section, and are then applied to the expander circuit to expand AF signals.

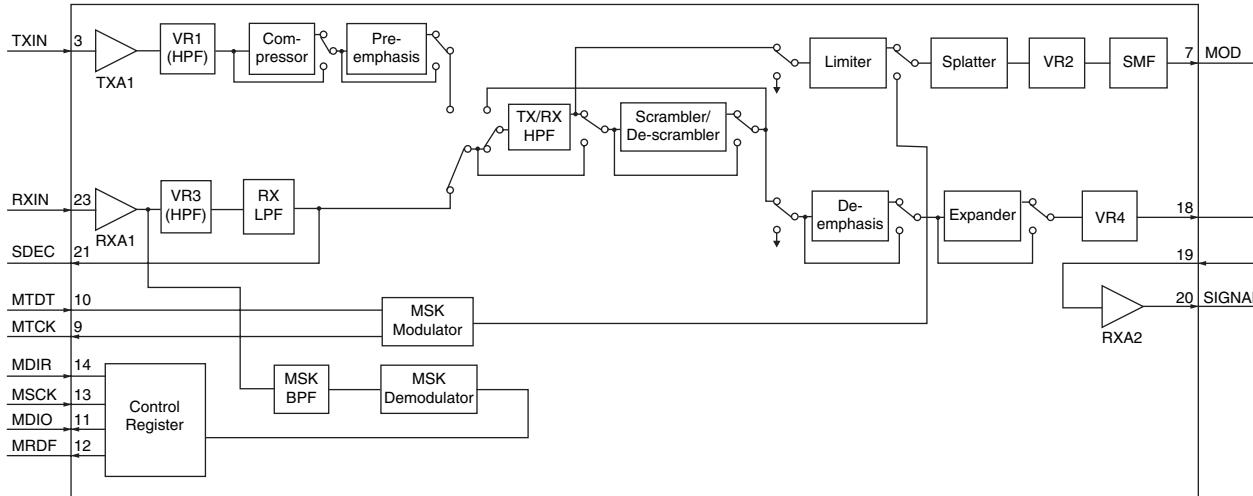
The output signals from the base band IC (IC2, pin 20) is applied to the AF amplifier circuit after amplified at the amplifier section.

#### (2) IN CASE OF TRANSMITTING

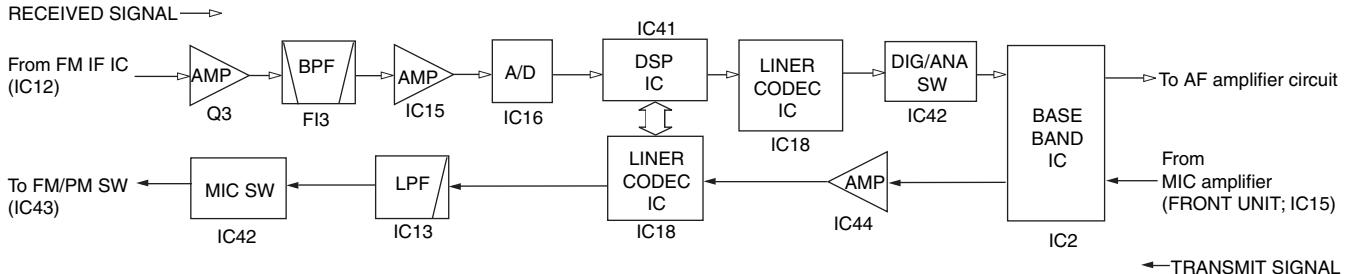
The audio signals from the microphone are applied to the base band IC (IC2, pin 3) via microphone amplifier (FRONT UNIT; IC5). The signals are amplified at the amplifier section, and are then applied to the compressor circuit to compress the audio signals. The signals pass through (or bypass) scrambler section, and are then applied to the limiter section after being passed through the high-pass filter.

The filtered signals pass through the splatter filter section, and are then applied to the modulation circuit (D12) via the FM/PM switch (IC43, pins 12–14) and D/A converter (IC8, pins 2, 3).

#### • BASE BAND IC BLOCK DIAGRAM



#### • DIGITAL MODE CIRCUITS



### 4-5-2 DIGITAL MODE CIRCUIT (IC-F1721D/F1821D only)

#### (1) IN CASE OF RECEIVING

A portion of the 2nd IF signal from the limiter amplifier section in the FM IF IC (IC12) output from pin 11 and is applied to the IF amplifier (Q3). The amplified signal is passed through a ceramic bandpass filter (F13) to suppress heterodyne noise, and amplified again at the digital IF amplifier (IC15, pins 1, 4). The amplified 2nd IF signal is applied to the A/D converter (IC16) to be converted into digital IF signal, then applied to the DSP IC (IC41). The DSP IC converts the digital IF signal into the digital audio signal.

The digital audio signal from DSP IC are converted into analog audio signals at the LINER CODEC IC (IC18) and output from pin 16.

The audio signals are applied to the base band IC (IC2, pin 23) after being pass through the DIG/ANA switch (IC42, pins 1, 15).

#### (2) IN CASE OF TRANSMITTING

The microphone signal from the base band IC (IC2, pin 7) are amplified at the MOD amplifier (IC44, pins 3, 4) and are then applied to the LINER CODEC IC (IC18, pin 2) to convert into the digital audio signal.

The digital audio signal is processed by DSP IC (IC41), and applied to the LINER CODEC IC (IC18) again.

The signal from the LINER CODEC IC (IC18, pin 15) is passed through the low-pass filter (IC13, pins 1, 3, 6, 7) and then applied to the PM/FM switch (IC43, pins 12–14) after pass through the microphone switch (IC42 pins 13, 14).

## 4-6 PORT ALLOCATIONS

### 4-6-1 MAIN CPU (MAIN UNIT; IC23)

Pin number	Port name	Description
1	DSDA	I/O port for data signal to the D/A converter (IC30 pin 6).
2	DAST	Outputs strobe signals to the D/A converter (IC8, pin 6).
10	SSO	Outputs serial data to the PLL IC (IC4, pin 15) and D/A converter (IC8, pin 8).
11	SCK	Outputs clock signal to the PLL IC (IC4 pin 14), D/A converter (IC8, pin 7), etc.
13	PLST	Outputs strobe signals to the PLL IC (IC4, pin 16).
15	DASW	Outputs control signal to the digital/analog switch (IC42). Low: While analog mode is selected.
16	TXC	Outputs the T8V regulator circuit (Q34) control signal. Low: During transmit.
17	TMUT	Outputs the R8V regulator circuit (Q30) control signal. Low: During receive.
18	AFON	Outputs control signal for AF mute circuit (Q28, Q29). High: While AF amplifier (IC38) is activated.
19	NWC	Outputs wide/narrow switch (D2, D4) control signal. High: When narrow band is selected.
20	DDSD	Input port for serial data from the DTMF decoder IC (IC6, pin 9).
21	DDAC	Outputs clock signals to the DTMF decoder IC (IC6, pin 10).
32	RMUT	Input port for the AF mute signal from the optional unit via J2. Low: While RX audio is muted.
33	MMUT	Input port for the microphone mute signal from the optional unit via J2. Low: While microphone audio is muted.
34–36	OPT1–OPT3	I/O ports for optional unit.
37	NOIS	Input port for the noise signal from the FM IF IC (IC9, pin 13).
38	POSW	Input port for the [①] switch. Low: While [①] switch is pushed.
39	DDST	Input port for DTMF detection signal from the DTMF decoder IC (IC6, pin 11).
40	IGSW	Input port for the remote power control signal from external connector, J7.
41	PWON	Outputs control signal for the power switch circuit (Q41, Q42). Low: While power ON.
43	SENC	Outputs single tone encoder signal.

Pin number	Port name	Description
44	BEEP	Outputs beep audio signals.
45	SDEC	Input port for single tone decode signal from the base band IC (IC2, pin 21).
46	CDEC	Input port for CTCSS/DTCS signal from the LPF (IC1, pin 7).
47	ULCK	Input port for the PLL unlock signal. Low: The PLL circuit is unlocked.
48	BATV	Input port for the connected battery for the low battery detection.
49	LVIN	Input port for the PLL lock voltage.
50	RSSI	Input port for the S-meter signal from the FM IF IC (IC12, pin 12).
51	TEMP	Input port for the transceiver's internal temperature detecting signal.
68	CLO	Outputs the data signal to the FRONT CPU (FRONT UNIT; IC3).
69	CLI	Input port for the data signal from the FRONT CPU (FRONT UNIT; IC3).
72	HORN	Outputs external device control signal. High: When matched 5/2 tone signals are received.
78	MTCK	Input port for transmitting MSK clock signal from the base band IC (IC2, pin 9).
79	NTXD	Outputs NMEA data signals for the connected unit via external connector (J7).
80	NRXD	Input port for NMEA data signals from the connected unit via external connector (J7).
88	DIM	Input port for the LCD backlight control signal from the external connector (J8). Low: While LCD backlight is dimmed.
89–91	CENC0–CENC2	Output the CTCSS/DTCS signals.
93	MTDT	Outputs the MSK data to the base band IC (IC2, pin 10).
94	MDIR	Outputs serial data control signal to the base band IC (IC2, pin 14).
95	MDIO	I/O port for the serial data signals from/to the base band IC (IC2, pin 11).
96	MSCK	Outputs clock signal for the base band IC (IC2, pin 13).
97	PMFM	Outputs the FM/PM switch (IC43, pin 11) control signal. High: While PM is selected.
98	ESDA	I/O port for data signals from/to the EEPROM (IC26, pin 5).
99	ESCL	Outputs clock signal to the EEPROM (IC26, pin 6).

#### 4-6-2 FRONT CPU (FRONT UNIT; IC3)

Pin number	Port name	Description															
7	RES	Input port for rest signal.															
19–22	KR0–KR3	Input ports for the 10-keypad. (IC-F1800 series only)															
28, 29	LIGT1, LIGT2	Output control signals for LCD backlight. <table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <td>LIGT1</td> <td>LIGT2</td> <td>LIGHT</td> </tr> <tr> <td>HIGH</td> <td>HIGH</td> <td>DIM</td> </tr> <tr> <td>HIGH</td> <td>LOW</td> <td>OFF</td> </tr> <tr> <td>LOW</td> <td>HIGH</td> <td>ON</td> </tr> <tr> <td>LOW</td> <td>LOW</td> <td>OFF</td> </tr> </table>	LIGT1	LIGT2	LIGHT	HIGH	HIGH	DIM	HIGH	LOW	OFF	LOW	HIGH	ON	LOW	LOW	OFF
LIGT1	LIGT2	LIGHT															
HIGH	HIGH	DIM															
HIGH	LOW	OFF															
LOW	HIGH	ON															
LOW	LOW	OFF															
47	LEDT	Outputs control signal for the TX LED.															
48	LEDR	Outputs control signal for the RX LED.															
51, 52	DICK, DIUP	Input ports for control signal from the dial (S9). (IC-F1700 series only)															
53, 54	KYUP, KYDN	Input ports for control signal from [▲], [▼] keys. (IC-F1800 series only)															
57	HANG	Input port for the microphone hanger detection signal. Low: When microphone on the hanger.															
58	PTT	Input port for the PTT switch of the connected microphone.															
59–63	KYP0–KYP4	Input ports for the programmable function keys (P0–P4).															

#### 4-6-4 D/A CONVERTER (MAIN UNIT; IC30)

Pin number	Port name	Description
1	T1	Outputs the bandpass filters (D23, D26) tuning signal.
2	T2	<ul style="list-style-type: none"> <li>• While receiving Outputs the bandpass filters (D17, D18) tuning signal.</li> <li>• While transmitting Outputs the TX power control signal which selects TX output power of HIGH, LOW1 or LOW2. The output signal is applied to the APC amplifier (IC37, pin 1).</li> </ul>
3	TXLVA	Outputs TX VCO lock voltage.
4	RXLVA	Outputs RX VCO lock voltage.

#### 4-6-3 D/A CONVERTER (MAIN UNIT; IC8)

Pin number	Port name	Description
2	SQL	Outputs AF signal to the squelch circuit (IC12, pin 8).
3	MOD	Outputs modulation signals to the VCO circuit.
10	TENC	Outputs CTCSS/DTCS signals.
11	BAL	Outputs deviation balance control signal.
14	BEPV	Outputs beep audio signals to the speaker via the AF amplifiers (IC34, IC38).
15	SIGNAL	Outputs AF signals to the speaker via the AF amplifiers (IC34, IC38).
22	TONE	Outputs single tone signal.
23	REF	Outputs reference oscillator control signal.

# SECTION 5 ADJUSTMENT PROCEDURES

## 5-1 PREPARATION

When adjusting IC-F1721/D,F1710,F1821/D,F1810, the optional CS-F1700 ADJ ADJUSTMENT SOFTWARE (Rev. 1.0 or later), JIG CABLE (modified OPC-1122 CLONING CABLE; see illustration on page 5-3) are required.

### ■ REQUIRED TEST EQUIPMENT

EQUIPMENT	GRADE AND RANGE	EQUIPMENT	GRADE AND RANGE
DC power supply	Output voltage : 13.6 (13.2) V DC Current capacity : 20 A or more	Audio generator	Frequency range : 300–3000 Hz Measuring range : 1–500 mV
Modulation analyzer	Frequency range : DC–600 MHz Measuring range : 0 to ±10 kHz	Attenuator	Power attenuation : 50 or 60 dB Capacity : 100 W
Frequency counter	Frequency range : 0.1–600 MHz Frequency accuracy : ±1 ppm or better Sensitivity : 100 mV or better	Standard signal generator (SSG)	Frequency range : 0.1–600 MHz Output level : 0.1 µV to 32 mV (–127 to –17 dBm)
Digital multimeter	Input impedance : 10 MΩ/V DC or more	AC millivoltmeter	Measuring range : 10 mV to 10 V
RF power meter	Measuring range : 1–75 W Frequency range : 100–800 MHz Impedance : 50 Ω SWR : Better than 1.2 : 1	Oscilloscope	Frequency range : DC–20 MHz Measuring range : 0.01–20 V
	External speaker	Input impedance : 4 Ω Capacity : 10 W or more	

### ■ SYSTEM REQUIREMENTS

- Microsoft® Windows® 98/98SE/Me/2000/XP
- RS-232C serial port (D-sub 9 pin)

### ■ ADJUSTMENT SOFTWARE INSTALLATION

- Quit all applications when Windows is running.
- Insert the CD into the appropriate CD drive.
- Double-click the "Setup.exe" contained in the 'CS-F1700 ADJ' folder in the CD drive.
- The "Welcome to the InstallShield Wizard for CS-F1700 ADJ" will appear. Click [Next>].
- The "Choose Destination Location" will appear. Then click [Next>] to install the software to the destination folder. (e.g. C:\Program Files\Icom\CS-F1700 ADJ)
- After the installation is completed, the "InstallShield Wizard Complete" will appear. Then click [Finish].
- Eject the CD.
- Program group 'CS-F1700 ADJ' appears in the 'Programs' folder of the start menu, and 'CS-F1700 ADJ' icon appears on the desk top screen.

### ■ BEFORE STARTING SOFTWARE ADJUSTMENT

Program the adjustment frequencies into the transceiver using with the CS-F1700 before starting the software adjustment. Otherwise, the transceiver can not start software adjustment.

**CAUTION! BACK UP** the originally programmed memory data in the transceiver before programming the adjustment frequencies.

When program the adjustment frequencies into the transceiver, the transceiver's memory data will be overwritten and lose original memory data at the same time.

Microsoft and Windows are registered trademarks of Microsoft Corporation in the U.S.A. and other countries.

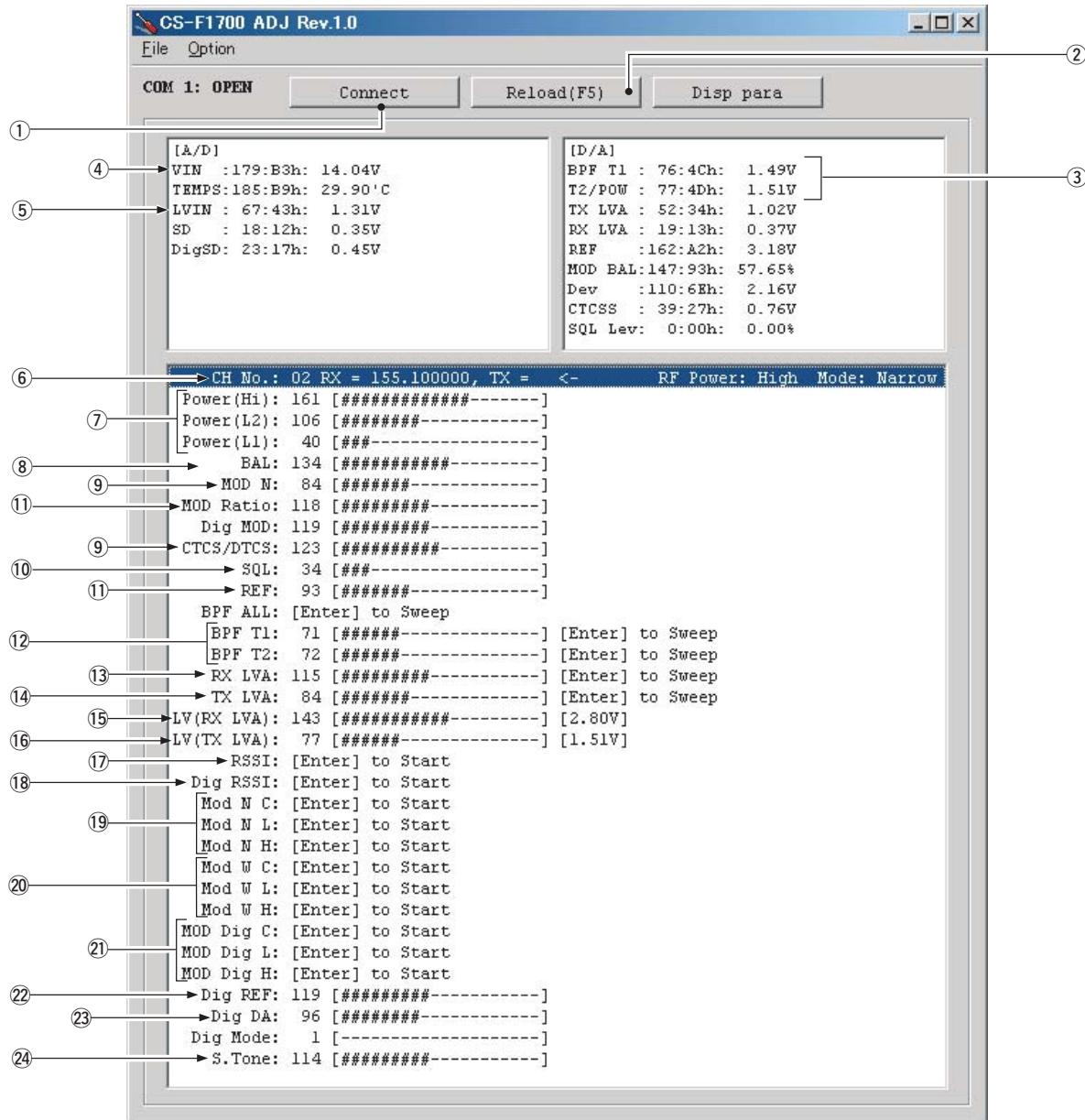
### ■ STARTING SOFTWARE ADJUSTMENT

- Connect the transceiver and PC with OPC-1122\* JIG CABLE.
- Turn the transceiver power ON.
- Boot up Windows, and click the program group 'CS-F1700 ADJ' in the 'Programs' folder of the [Start] menu, then CS-F1700 ADJ's window appears.
- Click 'Connect' on the CS-F1700 ADJ's window, then appears transceiver's up-to-date condition.
- Set or modify adjustment data as desired.

### • ADJUSTMENT FREQUENCY LIST

CH	FREQUENCY	CONDITIONS
1	155.000 MHz	TX power : Low1 Mode : Wide/Middle
2	155.000 MHz	TX power : Low2 Mode : Wide
3	155.000 MHz	TX power : High Mode : Wide
4	155.000 MHz	TX power : Low1 Mode : Narrow
5	155.000 MHz	TX power : Low1 Mode : Wide CTCSS : 151.4 Hz
6	155.000 MHz	TX power : Low1 Mode : Digital
7	174.000 MHz	TX power : Low1 Mode : Wide/Middle
8	174.000 MHz	TX power : Low1 Mode : Narrow
9	174.000 MHz	TX power : Low1 Mode : Digital
10	136.000 MHz	TX power : Low1 Mode : Wide/Middle
11	136.000 MHz	TX power : Low1 Mode : Narrow
12	136.000 MHz	TX power : Low1 Mode : Digital
13	136.000 MHz	TX power : Low1 Mode : Wide

• CS-F1700 ADJ'S SCREEN EXAMPLE

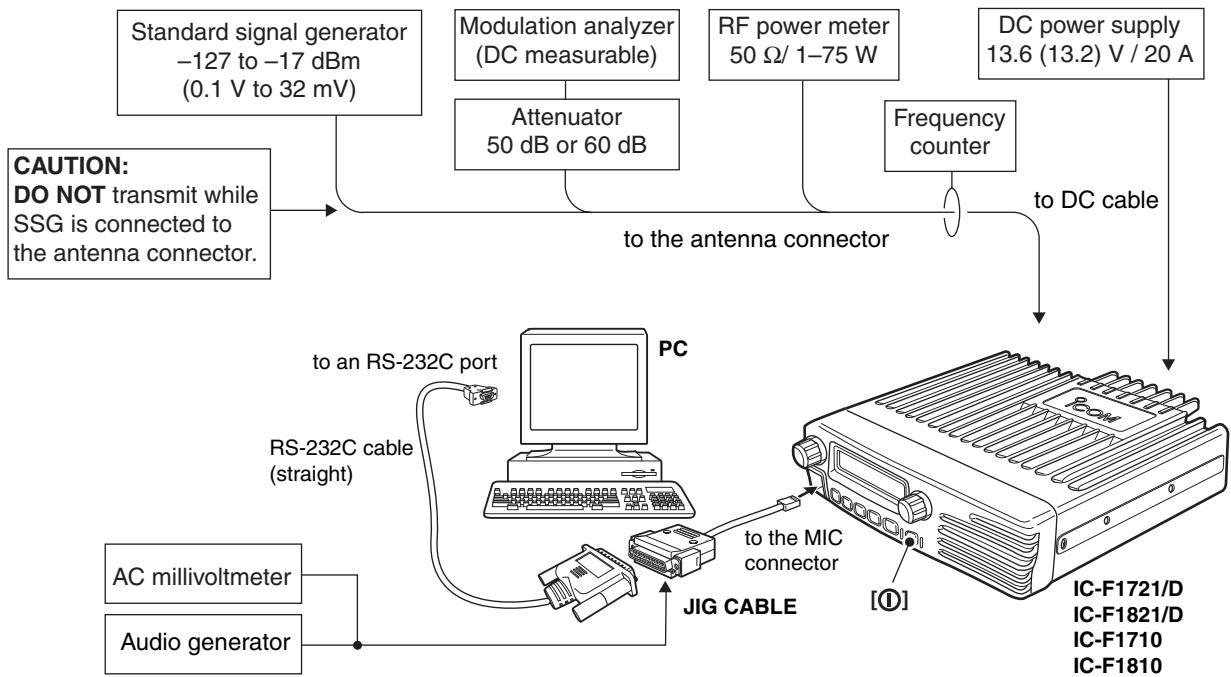


**NOTE:** The above values for settings are example only.

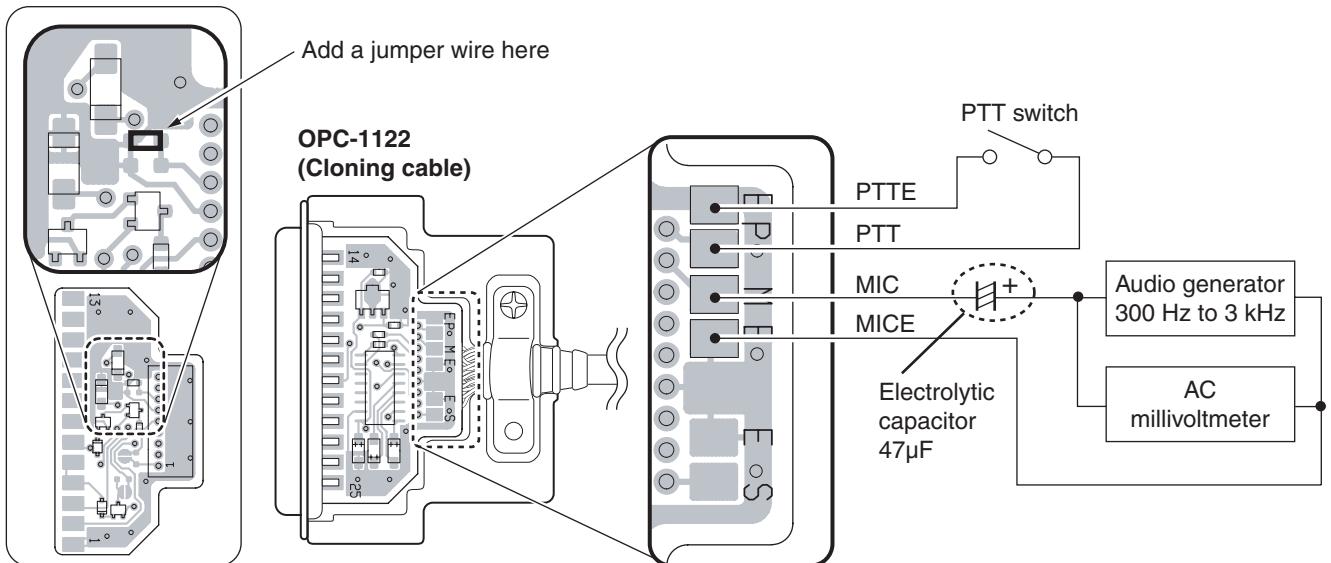
Each transceiver has its own specific values for each setting.

- |                                     |  |
|-------------------------------------|--|
| ①: Transceiver's connection state   | ⑬: PLL lock voltage for RX (automatic) |
| ②: Reload adjustment data           | ⑭: PLL lock voltage for TX (automatic) |
| ③: Receive sensitivity measurement  | ⑮: PLL lock voltage for RX (manual)    |
| ④: Connected DC voltage measurement | ⑯: PLL lock voltage for TX (manual)    |
| ⑤: PLL lock voltage measurement     | ⑰: S-meter adjustment                  |
| ⑥: Operating channel select         | ⑱: Digital RSSI                        |
| ⑦: RF output power                  | ⑲: Deviation (narrow)                  |
| ⑧: FM modulation balance (narrow)   | ⑳: Deviation (wide/middle)             |
| ⑨: CTCSS/DTCS deviation             | ㉑: Deviation (digital)                 |
| ⑩: Squelch level                    | ㉒: DSP frequency                       |
| ⑪: Reference frequency              | ㉓: Base band frequency                 |
| ⑫: Receive sensitivity (automatic)  | ㉔: 2/5 TONE deviation                  |

## • CONNECTION



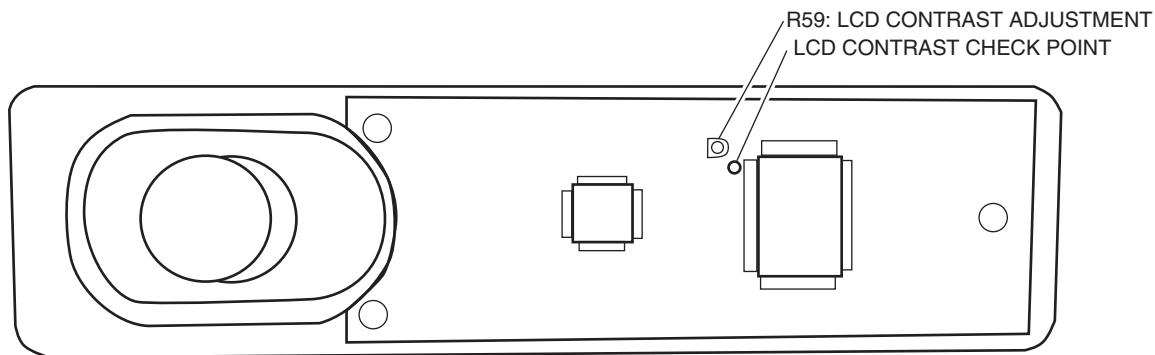
## • JIG CABLE



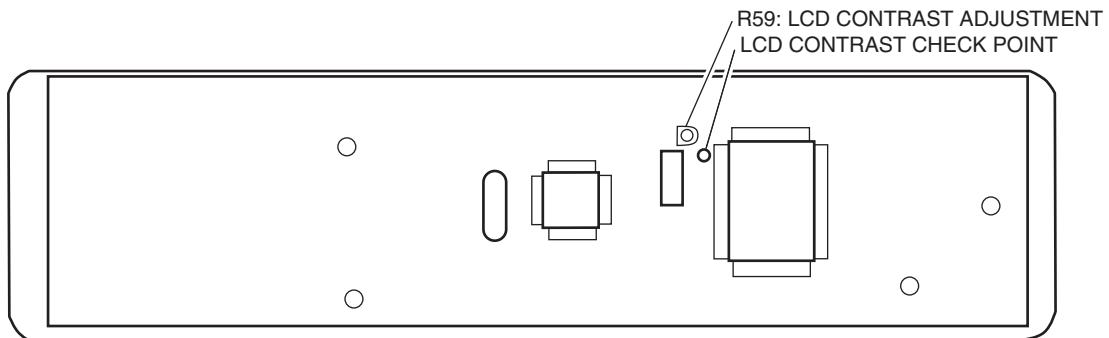
## 5-2 LCD CONTRAST ADJUSTMENT

ADJUSTMENT	ADJUSTMENT CONDITION	MEASUREMENT		VALUE	ADJUSTMENT	
		UNIT	LOCATION		UNIT	ADJUST
LCD CONTRAST	1 • Operating CH. : CH 1 • Preset LCD contrast : 64 (user set mode) • Receiving	FRONT A/B	Connect a digital multimeter or an oscilloscope to the check point "CONTRAST".	-2.0 V	FRONT A/B	R59

### • FRONT-A UNIT for IC-F1700 series



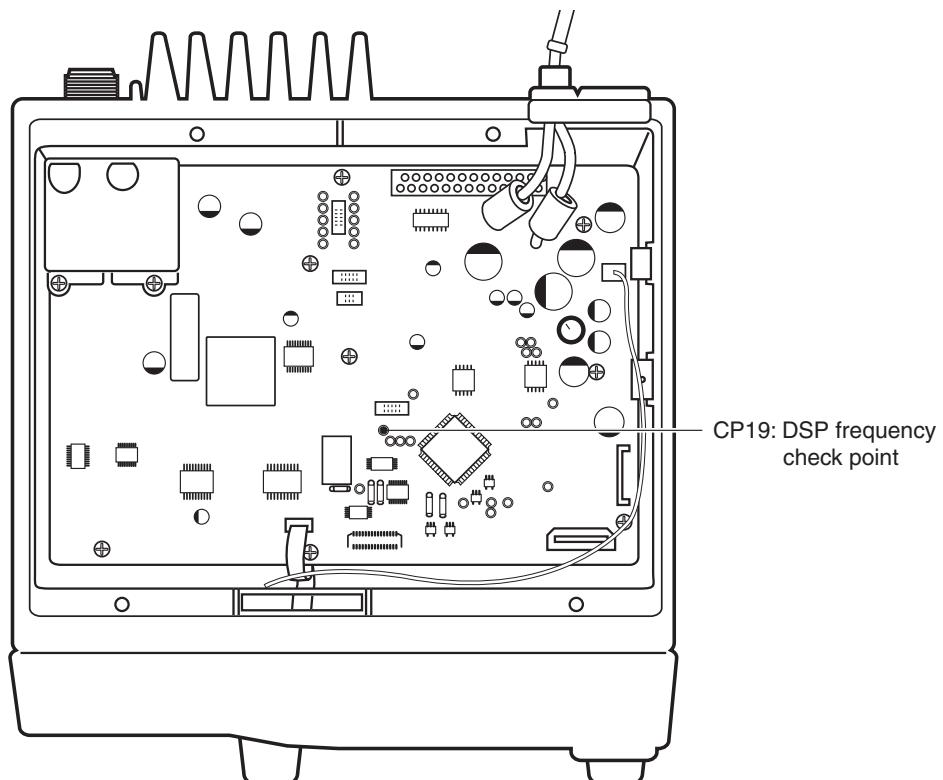
### • FRONT-B UNIT for IC-F1800 series



## 5-3 SOFT WARE ADJUSTMENT

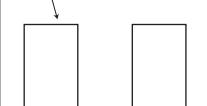
Select an operation using [ $\uparrow$ ] / [ $\downarrow$ ] keys, then set specified value using [ $\leftarrow$ ] / [ $\rightarrow$ ] keys on the connected computer keyboard.

ADJUSTMENT		ADJUSTMENT CONDITION	MEASUREMENT		VALUE
			UNIT	LOCATION	
PLL LOCK VOLTAGE [LV (RX LVA)] [LV (TX LVA)]	1	<ul style="list-style-type: none"> <li>• Operating CH. : CH 1</li> <li>• Preset LV(RX LVA) : 158 [3.10 V]</li> <li>• Receiving</li> </ul>	PC screen	Check the "LVIN" item on the CS-F1700 ADJ's screen.	3.10 V
	2	<ul style="list-style-type: none"> <li>• Operating CH. : CH 10</li> <li>• Preset LV(TX LVA) : 46 [0.90 V]</li> <li>• Transmitting</li> </ul>			0.90 V
<b>CONVENIENT:</b> The PLL lock voltage can be adjustment automatically. Set the cursor to "RX LVA"/"TX LVA" and then push [ENTER] key.					
REFERENCE FREQUENCY [REF]	3	<ul style="list-style-type: none"> <li>• Operating CH. : CH 7</li> <li>• Receiving</li> </ul>	PC screen	Check the "LVIN" item on the CS-F1700 ADJ's screen.	3.0–4.8 V (Verify)
	4	• Transmitting			2.0–3.0 V (Verify)
DSP FREQUENCY [Dig REF] (IC-F1721D/ F1821D only)	<ul style="list-style-type: none"> <li>• Operating CH. : CH 9</li> <li>• Connect an RF power meter or 50 <math>\Omega</math> dummy load to the antenna connector.</li> <li>• Transmitting</li> </ul>	Rear panel	MAIN unit	Loosely couple a frequency counter to the antenna connector.	174.000000 MHz
BASE BAND FREQUENCY [Dig DA] (IC-F1721D/ F1821D only)	<ul style="list-style-type: none"> <li>• Operating CH. : CH 9</li> <li>• Preset Dig Mode : 13</li> <li>• Connect an RF power meter or 50 <math>\Omega</math> dummy load to the antenna connector.</li> <li>• Transmitting</li> </ul>				12.288000 MHz
BASE BAND FREQUENCY [Dig DA] (IC-F1721D/ F1821D only)		Rear panel	Rear panel	Loosely couple a frequency counter to the antenna connector.	174.000000 MHz



## SOFTWARE ADJUSTMENT (Continued)

Select an operation using [ $\uparrow$ ] / [ $\downarrow$ ] keys, then set specified value using [ $\leftarrow$ ] / [ $\rightarrow$ ] keys on the connected computer keyboard.

ADJUSTMENT		ADJUSTMENT CONDITION	MEASUREMENT		VALUE
			UNIT	LOCATION	
OUTPUT POWER [Power (Hi)]	1	<ul style="list-style-type: none"> <li>Operating CH. : CH 3</li> <li>Transmitting</li> </ul>	Rear panel	Connect an RF power meter to the antenna connector.	25.0 W [25W] 50.0 W [50W]
[Power (L2)]	2	<ul style="list-style-type: none"> <li>Operating CH. : CH 2</li> <li>Transmitting</li> </ul>			10.0 W [25W] 25.0 W [50W]
[Power (L1)]	3	<ul style="list-style-type: none"> <li>Operating CH. : CH 1</li> <li>Transmitting</li> </ul>			2.5 W [25W] 5.0 W [50W]
MODULATION BALANCE [BAL]	1	<ul style="list-style-type: none"> <li>Operating CH. : CH 11</li> <li>Preset [MOD N] : 100</li> <li>No audio applied to the [MIC] connector.</li> <li>Set a modulation analyzer as:           <ul style="list-style-type: none"> <li>HPF : OFF</li> <li>LPF : 20 kHz</li> <li>De-emphasis : OFF</li> <li>Detector : (P-P)/2</li> </ul> </li> <li>Push [P0] while transmitting.</li> </ul>	Rear panel	Connect a modulation analyzer with an oscilloscope to the antenna connector through an attenuator.	 Set to square wave form
FM DEVIATION (NARROW) [MOD N C]	1	<ul style="list-style-type: none"> <li>Operating CH. : CH 4</li> <li>Connect an audio generator to the [MIC] connector and set as : 1.0 kHz/40 mVrms</li> <li>Set a Modulation analyzer as:           <ul style="list-style-type: none"> <li>HPF : OFF</li> <li>LPF : 20 kHz</li> <li>De- emphasis : OFF</li> <li>Detector : (P-P)/2</li> </ul> </li> <li>Transmitting</li> </ul>			
(NARROW) [MOD N L]	2	<ul style="list-style-type: none"> <li>Operating CH. : CH 11</li> <li>Transmitting</li> </ul>			
(NARROW) [MOD N H]	3	<ul style="list-style-type: none"> <li>Operating CH. : CH 8</li> <li>Transmitting</li> </ul>			
(WIDE) [MOD W C]	4	<ul style="list-style-type: none"> <li>Operating CH. : CH 1</li> <li>Transmitting</li> </ul>			
(WIDE) [MOD W L]	5	<ul style="list-style-type: none"> <li>Operating CH. : CH 10</li> <li>Transmitting</li> </ul>			
(WIDE) [MOD W H]	6	<ul style="list-style-type: none"> <li>Operating CH. : CH 7</li> <li>Transmitting</li> </ul>			
(MIDDLE) [MOD W C] ([EUR] only)	7	<ul style="list-style-type: none"> <li>Operating CH. : CH 1</li> <li>Transmitting</li> </ul>			
(MIDDLE) [MOD W L] ([EUR] only)	8	<ul style="list-style-type: none"> <li>Operating CH. : CH 10</li> <li>Transmitting</li> </ul>			
(MIDDLE) [MOD W H] ([EUR] only)	9	<ul style="list-style-type: none"> <li>Operating CH. : Ch 7</li> <li>Transmitting</li> </ul>			

## SOFTWARE ADJUSTMENT (Continued)

Select an operation using [↑] / [↓] keys, then set specified value using [←] / [→] keys on the connected computer keyboard.

ADJUSTMENT		ADJUSTMENT CONDITION	MEASUREMENT		VALUE								
			UNIT	LOCATION									
DIGITAL DEVIATION (Digital) [MOD Dig C] (IC-F1721D/ F1821D only)	1	<ul style="list-style-type: none"> <li>• Operating CH. : CH 6</li> <li>• Set a modulation analyzer as:           <table> <tr><td>HPF</td><td>: OFF</td></tr> <tr><td>LPF</td><td>: 20 kHz</td></tr> <tr><td>De- emphasis</td><td>: OFF</td></tr> <tr><td>Detector</td><td>: (P-P)/2</td></tr> </table> </li> <li>• Transmitting</li> </ul>	HPF	: OFF	LPF	: 20 kHz	De- emphasis	: OFF	Detector	: (P-P)/2	Rear panel	Connect a modulation analyzer to the antenna connector through an attenuator.	±2.85 kHz
HPF	: OFF												
LPF	: 20 kHz												
De- emphasis	: OFF												
Detector	: (P-P)/2												
(Digital) [MOD Dig L] (IC-F1721D/ F1821D only)	2	Operating CH. : CH 12 Transmitting	±2.85 kHz										
(Digital) [MOD Dig H] (IC-F1721D/ F1821D only)	3	Operating CH. : CH 9 Transmitting	±2.85 kHz										
CTCSS/DTCS DEVIATION [CTCSS/DTCS]	1	<ul style="list-style-type: none"> <li>• Operating CH. : CH 5</li> <li>• No audio applied to the [MIC] connector.</li> <li>• Set a modulation analyzer as:           <table> <tr><td>HPF</td><td>: OFF</td></tr> <tr><td>LPF</td><td>: 20 kHz</td></tr> <tr><td>De- emphasis</td><td>: OFF</td></tr> <tr><td>Detector</td><td>: (P-P)/2</td></tr> </table> </li> <li>• Transmitting</li> </ul>	HPF	: OFF	LPF	: 20 kHz	De- emphasis	: OFF	Detector	: (P-P)/2	Rear panel	Connect a modulation analyzer to the antenna connector through an attenuator.	±0.70 kHz
HPF	: OFF												
LPF	: 20 kHz												
De- emphasis	: OFF												
Detector	: (P-P)/2												
2TONE /5TONE /DTMF DEVIATION [S.Tone]	1	<ul style="list-style-type: none"> <li>• Operating CH. : CH 4</li> <li>• No audio applied to the [MIC] connector.</li> <li>• Set a modulation analyzer as:           <table> <tr><td>HPF</td><td>: OFF</td></tr> <tr><td>LPF</td><td>: 20 kHz</td></tr> <tr><td>De- emphasis</td><td>: OFF</td></tr> <tr><td>Detector</td><td>: (P-P)/2</td></tr> </table> </li> <li>• Push [P3] while transmitting.</li> </ul>	HPF	: OFF	LPF	: 20 kHz	De- emphasis	: OFF	Detector	: (P-P)/2	Rear panel	Connect a modulation analyzer to the antenna connector through an attenuator.	±1.50 kHz
HPF	: OFF												
LPF	: 20 kHz												
De- emphasis	: OFF												
Detector	: (P-P)/2												

## SOFTWARE ADJUSTMENT (continued)

- Select an operation using [ $\uparrow$ ] / [ $\downarrow$ ] keys, then set specified value using [ $\leftarrow$ ] / [ $\rightarrow$ ] keys on the connected computer keyboard.

ADJUSTMENT		ADJUSTMENT CONDITION	MEASUREMENT		VALUE								
			UNIT	LOCATION									
<b>NOTE:</b> Adjust the adjustment items as follows thoroughly in sequence.													
RX SENSITIVITY [BPF T1] [BPF T2] (Analog)	1	<ul style="list-style-type: none"> <li>Operating CH : CH 13</li> <li>Connect the SSG to the antenna connector and set as:           <table> <tr><td>Frequency</td><td>: 136.000 MHz</td></tr> <tr><td>Level</td><td>: 10 <math>\mu</math>V* (-87 dBm)</td></tr> <tr><td>Modulation</td><td>: 1 kHz</td></tr> <tr><td>Deviation</td><td>: <math>\pm</math>3.5 kHz</td></tr> </table> </li> <li>Receiving</li> </ul>	Frequency	: 136.000 MHz	Level	: 10 $\mu$ V* (-87 dBm)	Modulation	: 1 kHz	Deviation	: $\pm$ 3.5 kHz	PC screen	Connect the SINAD meter with a 4 $\Omega$ load to the [EXT SP] jack.	Minimum distortion level
Frequency	: 136.000 MHz												
Level	: 10 $\mu$ V* (-87 dBm)												
Modulation	: 1 kHz												
Deviation	: $\pm$ 3.5 kHz												
<b>CONVENIENT:</b> The BPF T1, BPF T2 can be adjustment automatically. ①-1: Set the cursor to "BPF ALL" and then push [ENTER] key. ①-2: The connected PC tunes BPF T1, T2 to peak levels. or ②-1: Set the cursor to one of BPF T1, T2 as desired. ②-2: Push [ENTER] key to start tuning. ②-3: Repeat ②-1 and ②-2 to perform additional BPF tuning.													
Digital RSSI [Dig RSSI] (IC-F1721D/ F1821D only)	1	<ul style="list-style-type: none"> <li>Operating CH. : CH 12</li> <li>Connect the SSG to the antenna connector and set as:           <table> <tr><td>Frequency</td><td>: 136.000 MHz</td></tr> <tr><td>Level</td><td>: 0.18 <math>\mu</math>V* (-122 dBm)</td></tr> <tr><td>Modulation</td><td>: OFF</td></tr> </table> </li> <li>Receiving</li> </ul>	Frequency	: 136.000 MHz	Level	: 0.18 $\mu$ V* (-122 dBm)	Modulation	: OFF	Push the [ENTER] key on the connected computer's keyboard to set "Dig RSSI" level.				
Frequency	: 136.000 MHz												
Level	: 0.18 $\mu$ V* (-122 dBm)												
Modulation	: OFF												
S-METER [RSSI]	1	<ul style="list-style-type: none"> <li>Operating CH. : CH 13</li> <li>Connect the SSG to the antenna connector and set as:           <table> <tr><td>Frequency</td><td>: 136.000 MHz</td></tr> <tr><td>Level</td><td>: 14 <math>\mu</math>V* (-84 dBm)</td></tr> <tr><td>Modulation</td><td>: OFF</td></tr> </table> </li> <li>Receiving</li> </ul>	Frequency	: 136.000 MHz	Level	: 14 $\mu$ V* (-84 dBm)	Modulation	: OFF	Push the [ENTER] key on the connected computer's keyboard to set "S3" level.				
Frequency	: 136.000 MHz												
Level	: 14 $\mu$ V* (-84 dBm)												
Modulation	: OFF												
2	<ul style="list-style-type: none"> <li>Set the SSG as: Level : 0.45 <math>\mu</math>V* (-114 dBm)</li> <li>Receiving</li> </ul>	Push the [ENTER] key on the connected computer's keyboard to set "S1" level.											
SQUELCH LEVEL [SQL]	1	<ul style="list-style-type: none"> <li>Operating CH. : CH 2</li> <li>Connect the SSG to the antenna connector and set as:           <table> <tr><td>Frequency</td><td>: 136.000 MHz</td></tr> <tr><td>Level</td><td>: 0.2 <math>\mu</math>V* (-121 dBm)</td></tr> <tr><td>Modulation</td><td>: OFF</td></tr> </table> </li> <li>Receiving</li> </ul>	Frequency	: 136.000 MHz	Level	: 0.2 $\mu$ V* (-121 dBm)	Modulation	: OFF	Rear panel	Connect speaker to the [EXT SP] jack.	Set SQL level to close squelch. Then set SQL level at the point where the audio signals just appears.		
Frequency	: 136.000 MHz												
Level	: 0.2 $\mu$ V* (-121 dBm)												
Modulation	: OFF												

\*The output level of the standard signal generator (SSG) is indicated as the SSG's open circuit.

## SECTION 6 PARTS LIST

### [REPLACEMENT UNITS]

ORDER NO.	UNIT NAME	
0327810101	U F1721 #01 FRONT-A	[F1721/D], [F1710]
0327811102	U F1821 #11 FRONT-B	[F1821/D], [F1810]

### [FRONT-A UNIT] (for IC-F1700 series)

REF NO.	ORDER NO.	DESCRIPTION	M.	H/V LOCATION
R42	7030005120	S.RES ERJ2GEJ 102 X (1 kΩ)	B	60.6/7.8
R43	7030005120	S.RES ERJ2GEJ 102 X (1 kΩ)	B	97.6/12.6
R44	7030005010	S.RES ERJ2GEJ 681 X (680 Ω)	B	104.8/12.5
R47	7030005050	S.RES ERJ2GEJ 103 X (10 kΩ)	B	83.4/34.2
R48	7030005090	S.RES ERJ2GEJ 104 X (100 kΩ)	B	74.9/29.4
R49	7030005090	S.RES ERJ2GEJ 104 X (100 kΩ)	B	75.8/29.6
R50	7030005090	S.RES ERJ2GEJ 104 X (100 kΩ)	B	76.7/29.9
R51	7030005090	S.RES ERJ2GEJ 104 X (100 kΩ)	B	77.6/30.2
R52	7030005090	S.RES ERJ2GEJ 104 X (100 kΩ)	B	78.5/29.9
R55	7510001470	S.TMR NTCG20 4AG 473JT		82.3/25.3
R56	7030005120	S.RES ERJ2GEJ 102 X (1 kΩ)	B	80.8/26.7
R57	7030003810	S.RES ERJ3GEYJ 125 V (1.2 MΩ)	B	57.9/33.2
R58	7030003810	S.RES ERJ3GEYJ 125 V (1.2 MΩ)	B	54.2/29.8
R59	7310002820	S.TRI RV-158 (RH03A3AS5) 474		55/32.2
R60	7030005240	S.RES ERJ2GEJ 473 X (47 kΩ)	B	14.5/10.7
R61	7030005090	S.RES ERJ2GEJ 104 X (100 kΩ)	B	19.7/8.6
R62	7030004980	S.RES ERJ2GEJ 101 X (100 Ω)	B	21.3/8.6
R63	7030005160	S.RES ERJ2GEJ 105 X (1 MΩ)	B	26.8/4.7
R64	7030005220	S.RES ERJ2GEJ 223 X (22 kΩ)	B	26.5/10.2
R65	7030007290	S.RES ERJ2GEJ 222 X (2.2 kΩ)	B	28.2/9.3
R66	7030009290	S.RES ERJ2GEJ 562 X (5.6 kΩ)	B	29.9/9.3
R67	7030009280	S.RES ERJ2GE 391 X	B	24.7/10.2
R68	7030007300	S.RES ERJ2GEJ 332 X (3.3 kΩ)	B	24.7/9.3
R69	7030005050	S.RES ERJ2GEJ 103 X (10 kΩ)	B	81.9/33.3
R70	7410001130	S.ARY EXB28V102JX		65.2/19.9
R71	7410001130	S.ARY EXB28V102JX		65.6/17
R72	7030005090	S.RES ERJ2GEJ 104 X (100 kΩ)	B	83.7/27.6
R73	7030005090	S.RES ERJ2GEJ 104 X (100 kΩ)	B	21.8/30.1
R74	7030005090	S.RES ERJ2GEJ 104 X (100 kΩ)	B	21.7/13.3
R75	7030005090	S.RES ERJ2GEJ 104 X (100 kΩ)	B	51.1/23.4
R76	7030005090	S.RES ERJ2GEJ 104 X (100 kΩ)	B	73/30.1
R77	7030005090	S.RES ERJ2GEJ 104 X (100 kΩ)	B	18.1/8.6
D1	1790000620	S.DIO MA77 (TX)	B	82.2/15.3
D4	1790001250	S.DIO MA2S111-(TX)	B	60/31.3
D5	1790000950	S.ZEN MA8056-M (TX)	B	22.7/28.7
D6	1790000950	S.ZEN MA8056-M (TX)	B	22.7/32.6
D7	1790000950	S.ZEN MA8056-M (TX)	T	19.3/16
D8	1750000550	S.DIO 1SS355 TE-17	B	86.7/12.6
D9	1750000130	S.DIO DA204U T106	B	59.1/9.9
D10	1750000130	S.DIO DA204U T106	B	56.5/9.9
D11	1750000130	S.DIO DA204U T106	B	52.4/9.6
D12	1790001250	S.DIO MA2S111-(TX)	B	69.6/29.5
X1	6050009520	S.XTL CR-520 (19.6608 MHz+)	B	86.6/20.5
L1	6200003640	S.COL MLF1608E 100K-T	B	12.3/9.7
R4	7030008010	S.RES ERJ2GEJ 123 XΩ(12 kΩ)	B	83.4/13.4
R5	7030008010	S.RES ERJ2GEJ 123 X (12 kΩ)	B	82.9/16.7
R6	7030005160	S.RES ERJ2GEJ 105 X (1 MΩ)	B	82.4/20.8
R7	7030008010	S.RES ERJ2GEJ 123 X (12 kΩ)	B	81.1/17
R8	7030005530	S.RES ERJ2GEJ 100 X (10 Ω)	B	81.1/20.8
R9	7030005090	S.RES ERJ2GEJ 104 X (100 kΩ)	B	53.5/21.1
R12	7030005090	S.RES ERJ2GEJ 104 X (100 kΩ)	B	59.5/29.6
R14	7030005090	S.RES ERJ2GEJ 104 X (100 kΩ)	B	62.3/32
R15	7030005090	S.RES ERJ2GEJ 104 X (100 kΩ)	B	59.8/27.2
R16	7030007300	S.RES ERJ2GEJ 332 X (3.3 kΩ)	B	59.5/33
R18	7030005220	S.RES ERJ2GEJ 223 X (22 kΩ)	B	61.3/25.2
R19	7030009280	S.RES ERJ2GE 391 X	B	67.3/10.6
R20	7030005240	S.RES ERJ2GEJ 473 X (47 kΩ)	T	18.6/14.6
R21	7030005090	S.RES ERJ2GEJ 104 X (100 kΩ)	B	21.8/31.2
R22	7030009140	S.RES ERJ2GEJ 272 X (2.7 kΩ)	B	67.8/11.6
R24	7030005050	S.RES ERJ2GEJ 103 X (10 kΩ)	B	28.3/17.9
R25	7030007290	S.RES ERJ2GEJ 222 X (2.2 kΩ)	B	26.5/11.1
R26	7030007290	S.RES ERJ2GEJ 222 X (2.2 kΩ)	B	24.8/16.5
R28	7030005220	S.RES ERJ2GEJ 223 X (22 kΩ)	B	26.5/12
R29	7030005050	S.RES ERJ2GEJ 103 X (10 kΩ)	B	26.7/17.9
R30	7030005120	S.RES ERJ2GEJ 102 X (1 kΩ)	B	17.6/16.1
R31	7030005120	S.RES ERJ2GEJ 102 X (1 kΩ)	B	12.1/21.1
R32	7030005120	S.RES ERJ2GEJ 102 X (1 kΩ)	B	11.7/19.7
R33	7030009160	S.RES ERJ2GEJ 181 X (180 Ω)	B	50.9/4.8
R34	7030009160	S.RES ERJ2GEJ 181 X (180 Ω)	B	65.1/8.5
R35	7210003050	VAR EVU-F2FKF3 B14 (10 kΩ)		
R36	7030009160	S.RES ERJ2GEJ 181 X (180 Ω)	B	64.1/8.4
R37	7030009160	S.RES ERJ2GEJ 181 X (180 Ω)	B	63.2/8.9
R38	7030005090	S.RES ERJ2GEJ 104 X (100 kΩ)	B	86.9/11.2
R39	7030005240	S.RES ERJ2GEJ 473 X (47 kΩ)	B	88.6/13.9
R40	7030005120	S.RES ERJ2GEJ 102 X (1 kΩ)	B	51.7/6.9
R41	7030005120	S.RES ERJ2GEJ 102 X (1 kΩ)	B	54.4/8.8

M.=Mounted side (T: Mounted on the Top side, B: Mounted on the Bottom side)  
 S.=Surface mount



















**[MAIN UNIT]**

REF NO.	ORDER NO.	DESCRIPTION		M.	H/V LOCATION
J5	6450000140	CNR	HSJ0807-01-010		
J6	6510014960	S.CNR	B2B-ZR-SM3-TF	T	150.3/83.8
J7	6510021300	S.CNR	52365-1091	T	88/77.7
J8	6510019250	S.CNR	B11B-ZR-SM3-TF	T	155.1/25.9
J10	6510019270	S.CNR	52365-0691	T	88/71
J11	6510023210	CNR	CD6125SA1J0 <CVI>		
J13	6510021300	S.CNR	52365-1091	T	84.9/93.5
W2	7120000470	JMP	ERDS2T0		
W3	8900013680	CBL	OPC-1414 <CMi>		
EP1	6910015600	S.BEA	ACZ1005Y-241 (240 Ω)	T	51.3/33.2
EP4	6910015370	S.BEA	ACZ1005Y-102-T	T	47.4/22.3
EP5	6910015370	S.BEA	ACZ1005Y-102-T	B	83.9/45.7
EP6	6910015370	S.BEA	ACZ1005Y-102-T	B	57.7/51.4
EP7	6910011560	BEA	HF70BB4.5X5X1.6		
EP8	6910011560	BEA	HF70BB4.5X5X1.6		
EP9	6910010280	BEA	HF70BB9.5X10.4X4.9		
EP10	6910010280	BEA	HF70BB9.5X10.4X4.9		

**[CHASSIS UNIT]**

REF NO.	ORDER NO.	DESCRIPTION		M.	H/V LOCATION
J1	6510004880	CNR	MR-DS-E 01		

M.=Mounted side (T: Mounted on the Top side, B: Mounted on the Bottom side)  
S.=Surface mount

## SECTION 7 MECHANICAL PARTS AND DISASSEMBLY

### [CHASSIS PARTS]

REF. NO.	ORDER NO.	DESCRIPTION	QTY.
J1	6510004880	Connector MR-DS-E 01	1
MP1	8010019800	2781 chassis	1
MP2	8110008270	2781 cover	1
MP3	8810008660	Screw PH BT M3 × 8 NI-ZU	12
MP4	8810008660	Screw PH BT M3 × 8 NI-ZU	2
MP5	8810008660	Screw PH BT M3 × 8 NI-ZU	2
MP6	8810009990	Screw PH BT M3 × 8 ZK	2
MP7	8810009990	Screw PH BT M3 × 8 ZK	4
MP8	8930064590	Plate 2781 D-SUB PLATE	1
MP9	8510016740	Case 2781 FILTER CASE Y755	1
MP10	8930048550	2177 clip	1
MP11	8930048520	2156 clip	1
MP12	8810009990	Screw PH BT M3 × 8 ZK	2

### [FRONT-A UNIT] (IC-F1700 Series)

REF. NO.	ORDER NO.	DESCRIPTION	QTY.
W1	8900013690	Cable OPC-1425 (N=12, L=92)	1
W2	8900013700	Cable OPC-1426	1
EP1	8930065150	LCD contact SRCN-2781-SP-N-W	2
MP1	8930064250	2781 angle Y754	1
MP2	8930064190	2781 front key	1
MP3	8210021430	2781 front panel assembly	1
MP4	8930064220	2781 knob rubber	1
MP5	8930064260	2781 LCD holder Y753	1
MP7	8210021190	2781 reflector	1
MP9	8610012160	Knob N324	1
MP10	8610012150	Knob N325	1
MP11	8810008660	Screw PH BT M3 × 8 NI-ZU	3
MP12	8810008660	Screw PH BT M3 × 8 NI-ZU	2
MP16	8930051500	Seal O-ring (AB)	1
MP18	8830000030	VR nut (C)	1
MP19	8930065250	2781 A-lens	1
MP20	8930065240	2781 B-lens	1
SP1	2510001290	Speaker C062SB504-11	1

### [FRONT-B UNIT] (IC-F1800 Series)

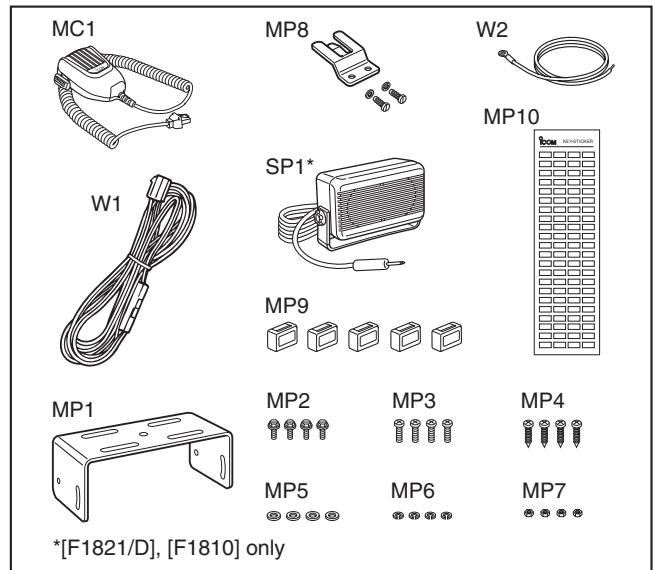
REF. NO.	ORDER NO.	DESCRIPTION	QTY.
W1	8900013690	Cable OPC-1425 (N=12, L=92)	1
EP1	8930065150	LCD contact SRCN-2781-SP-N-W	2
MP1	8930064190	2781 front key	1
MP2	8930064220	2781 knob rubber	1
MP3	8930064260	2781 LCD holder Y753	1
MP5	8210021190	2781 reflector	1
MP6	8930064370	2781 T-angle	1
MP7	8210021440	2781 T-front panel assembly	1
MP8	8930064520	2781 UP/DOWN key	1
MP10	8930064380	2781 10-key	1
MP11	8610012160	Knob N324	1
MP12	8810008760	Screw PH BT M2 × 8 NI-ZU	6
MP14	8930064890	2781 T-sheet	1
MP17	8930065250	2781 A-lens	1
MP18	8930065240	2781 B-lens	1
MP20	8930065170	2781 LED sheet	2

### [MAIN UNIT]

REF. NO.	ORDER NO.	DESCRIPTION	QTY.
W3	8900013680	Cable OPC-1414 <CMI>T	1
J11	6510023210	CD6125SA1J0	1
EP9	6910010280	Bead HF70BB9.5 × 10.4 × 4.9	1
EP10	6910010280	Bead HF70BB9.5 × 10.4 × 4.9	1
MP1	8510014940	2601 VCO case Y641 (Tip)	1
MP2	8510014950	2601 VCO cover Y642	1
MP4	8510014890	2577 DBM case	1
MP5	8930065060	2781 M-plate	1
MP6	8510016820	2781 shield plate	1

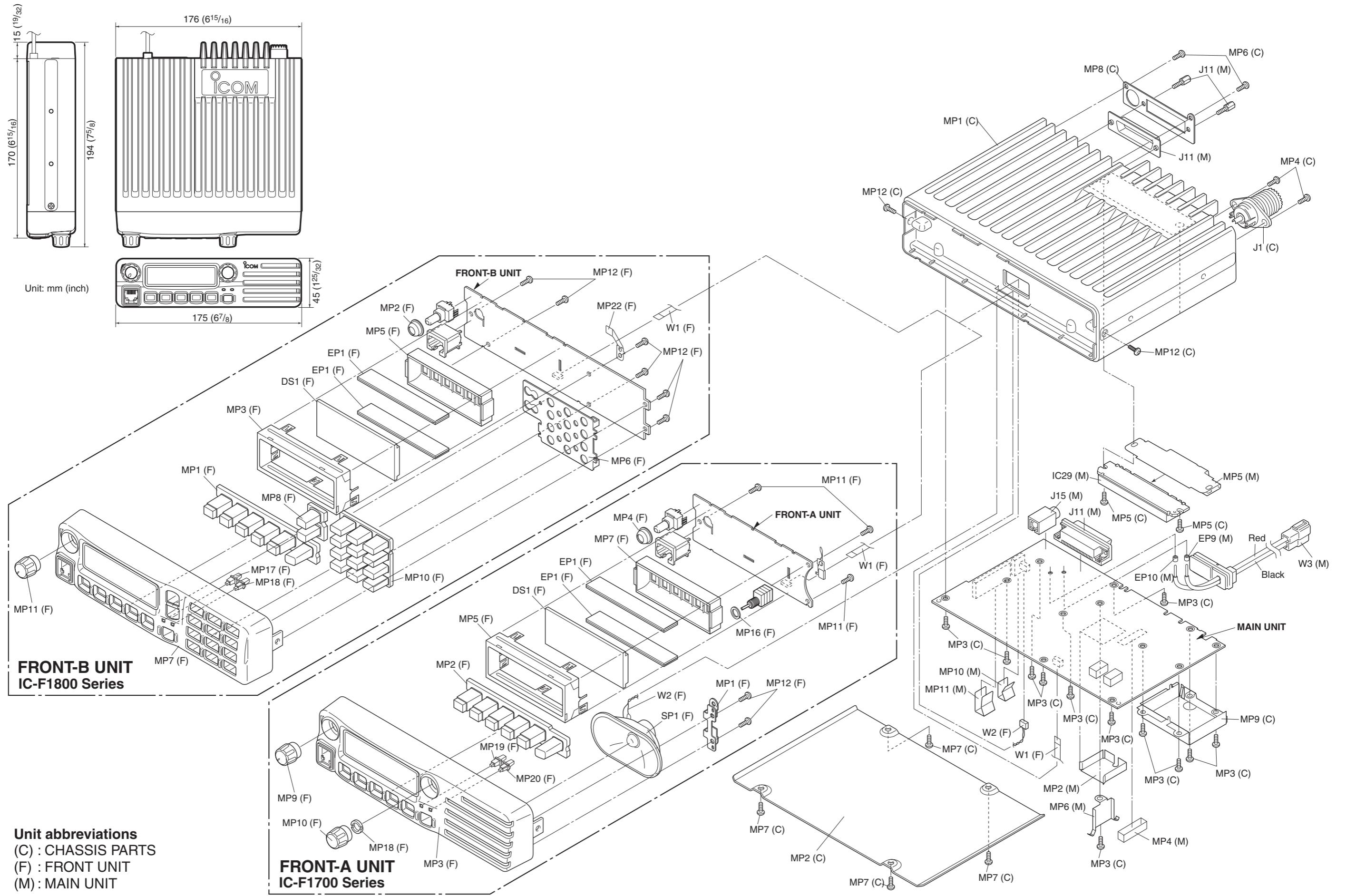
### [ACCESSORIES]

REF. NO.	ORDER NO.	DESCRIPTION	QTY.
W1	8900010990	DC power cable OPC-1132 [USA]	1
	8900011780	DC power cable OPC-1194 [EUR], [GEN]	1
W2	8900000730	Microphone hanger cable OPC-049	1
MC1	Optional product	Microphone HM-100N [EUR], [GEN]	1
	Optional product	Microphone HM-148 [USA]	1
MP1	8010019880	2781 mounting bracket assembly	1
MP2	8820000530	Screw bracket bolts M4 × 8 NI	4
MP3	8810000470	Screw M5 × 12 (+ -)	4
MP4	8810000950	Screw (PH) A0 M5 × 16	4
MP5	8850000150	Flat washer M5 NI BS	4
MP6	8850000390	Spring washer M5	4
MP7	8830000120	Nut M5	4
MP8	6910004210	731 mic hanger assembly	1
MP9	8930064670	2781 key cap	5
MP10	8930064820	2781 key sheet	1
SP1	Optional product	Speaker SP-22 [F1821/D], [F1810] only	1



#### Screw abbreviations

A0, B0, BT: Self-tapping  
 PH: Pan head  
 NI: Nickel  
 SUS: Stainless  
 NI-ZU: Nickel-Zinc



## SECTION 8 SEMI-CONDUCTOR INFORMATION

### • TRANSISTOR AND FET'S

2SA1577 T106 Q (S mbol: HQ)	2SB1132 Q (S mbol: BAQ)	2SC3356 T1B R25 (S mbol: R25)	2SC4116 BL (S mbol: LL)	2SC4215 O (S mbol: QO)
2SC4226 T1 R25 (S mbol: R25)	2SC5107 O (S mbol: MFO)	2SD1664 T100Q (S mbol: DAQ)	2SJ144 GR (S mbol: VG)	2SJ377 (S mbol: 4L)
2SK880 Y (S mbol: XY)	2SK1829 (S mbol: K1)	3SK293 (S mbol: UF)	DTA114EUA T106 (S mbol: U73)	DTA144EUA T106 (S mbol: 16)
DTC114EUA T106 (S mbol: 04)	DTC114TUA T106 (S mbol: 04)	DTC144EUA T106 (S mbol: 26)	DTC363 EK (S mbol: H27)	PMBFJ310 (S mbol: 50*)
XP1214 (S mbol: 9H)	XP6501 AB (S mbol: 5N)			

### • DIODES

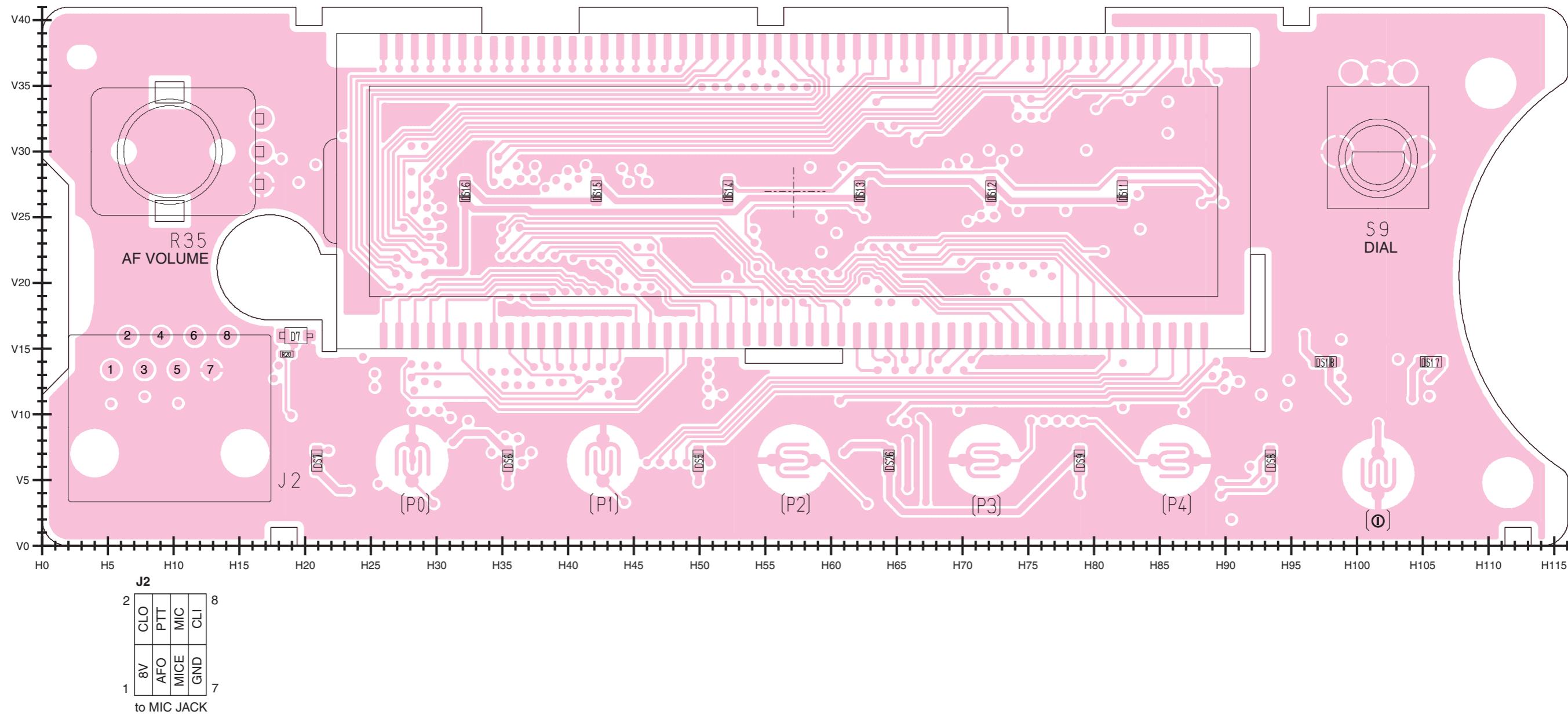
1SS355 (S mbol: A)	1SS375-TL (S mbol: FH)	1SV239 (S mbol: TC)	DA204U (S mbol: K)	DA221 TL (S mbol: K)
DAN202K T146 (S mbol: N)	DAN202U T106 (S mbol: N)	DAN222TL (S mbol: N-4)	DAP202U T106 (S mbol: P)	DSA3A1 (S mbol: Green)
HSB88WSTR (S mbol: Silver line)	HVC321B1 (S mbol: V8)	HVC350B (S mbol: B0)	HVC375B (S mbol: B8)	HVC376B (S mbol: B9)
MA2S111 (S mbol: A)	MA2S728 (S mbol: B)	MA77 (S mbol: 4B)	MA8056 M (S mbol: 5-6)	RB886G T2R (S mbol: C)
UM9401F (S mbol: none)	XB15A407 (S mbol: None)			

## SECTION 9 BOARD LAYOUTS

### 9-1 FRONT-A UNIT (for IC-F1700 Series)

•TOP VIEW

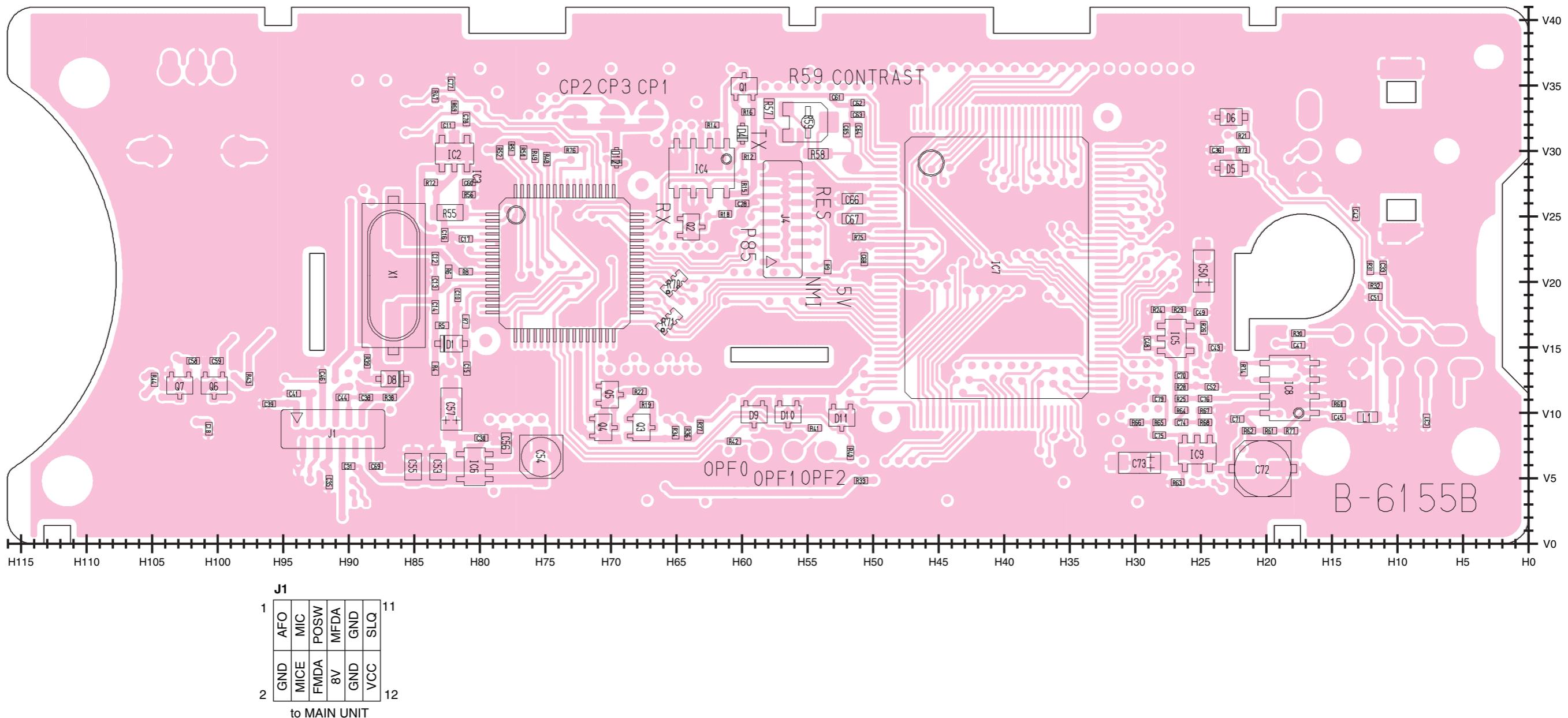
The combination of this page and the next page shows  
the unit layout in the same configuration as the actual  
P.C. Board.



## FRONT-A UNIT

• BOTTOM VIEW (for IC-F1700 series)

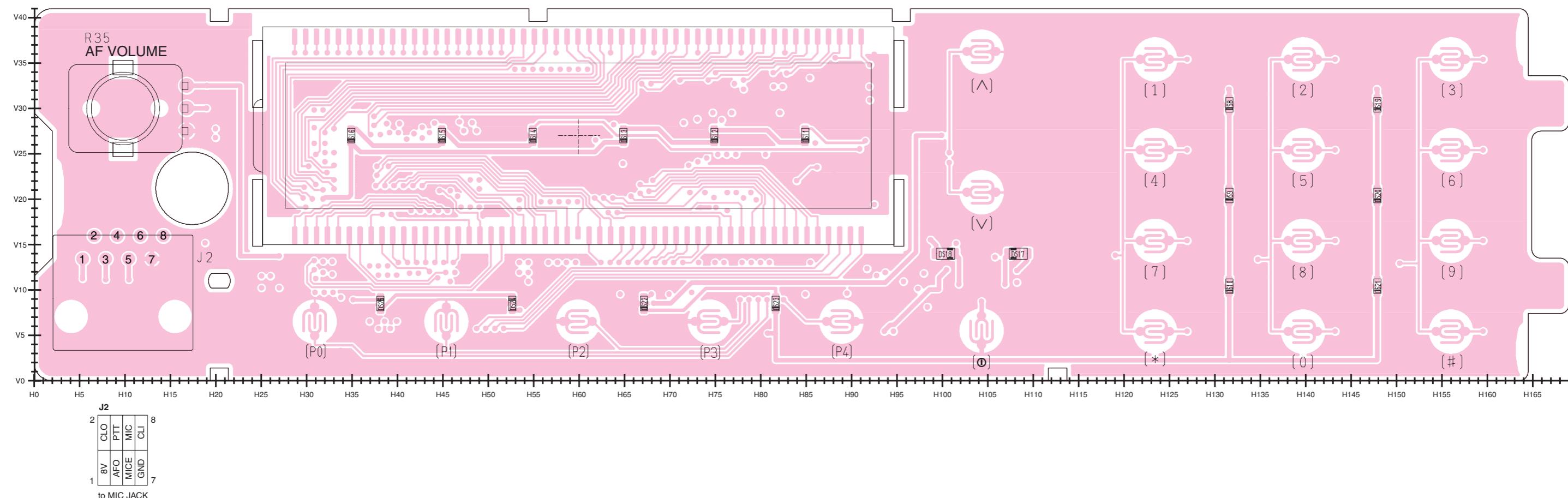
The combination of this page and the previous page shows the unit layout in the same configuration as the actual P.C. Board.



## 9-2 FRONT-B UNIT (for IC-F1800 Series)

### • TOP VIEW

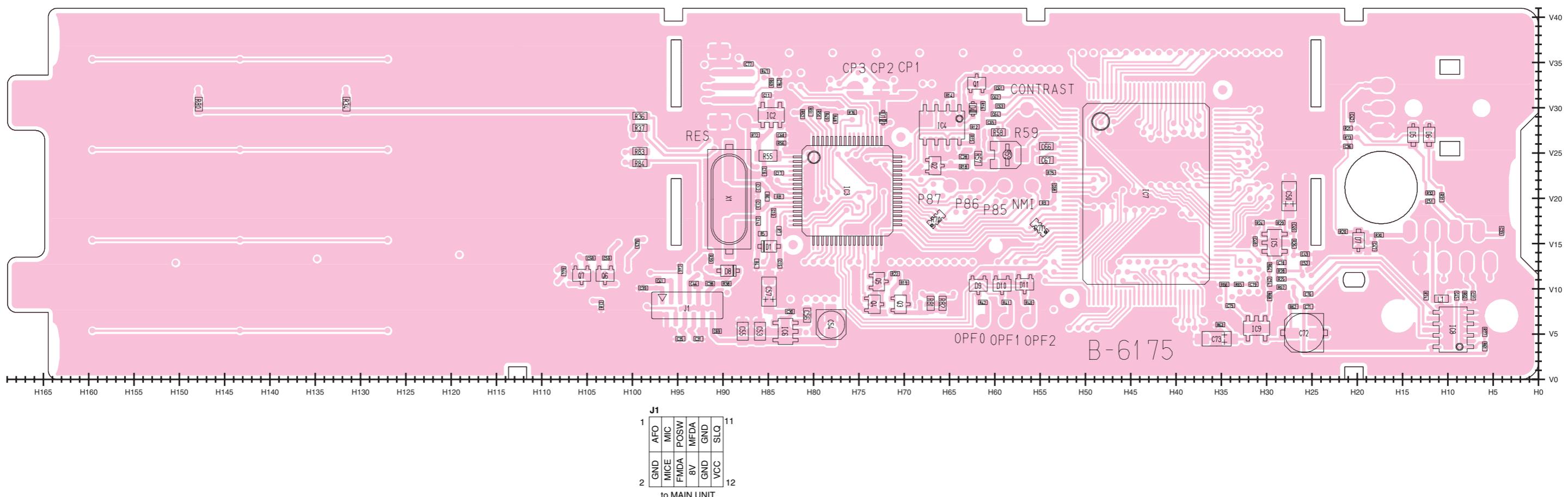
The combination of this page and the next page shows the unit layout in the same configuration as the actual P.C. Board.



## FRONT-B UNIT

• BOTTOM VIEW (for IC-F1800 series)

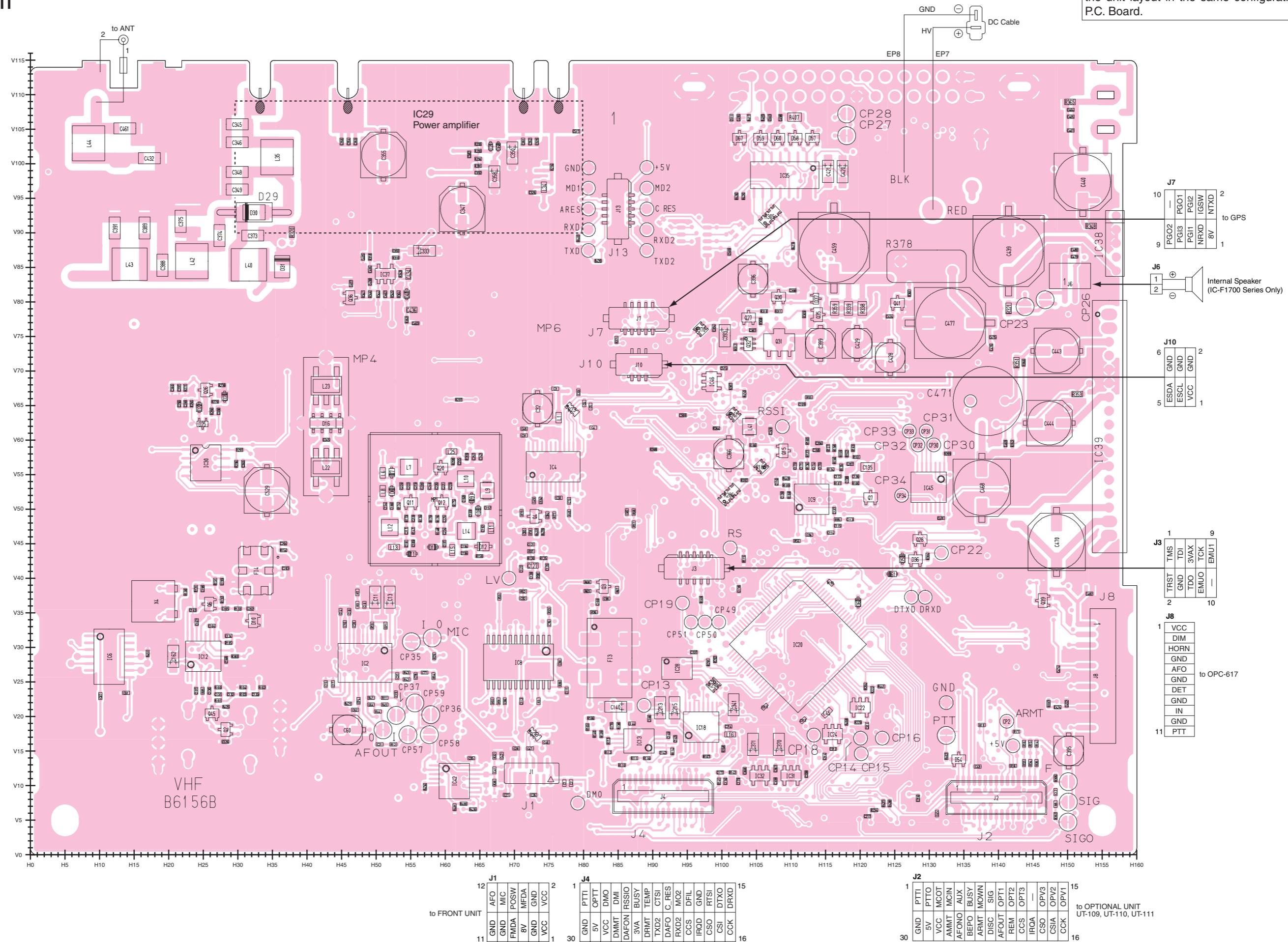
The combination of this page and the previous page shows the unit layout in the same configuration as the actual P.C. Board.



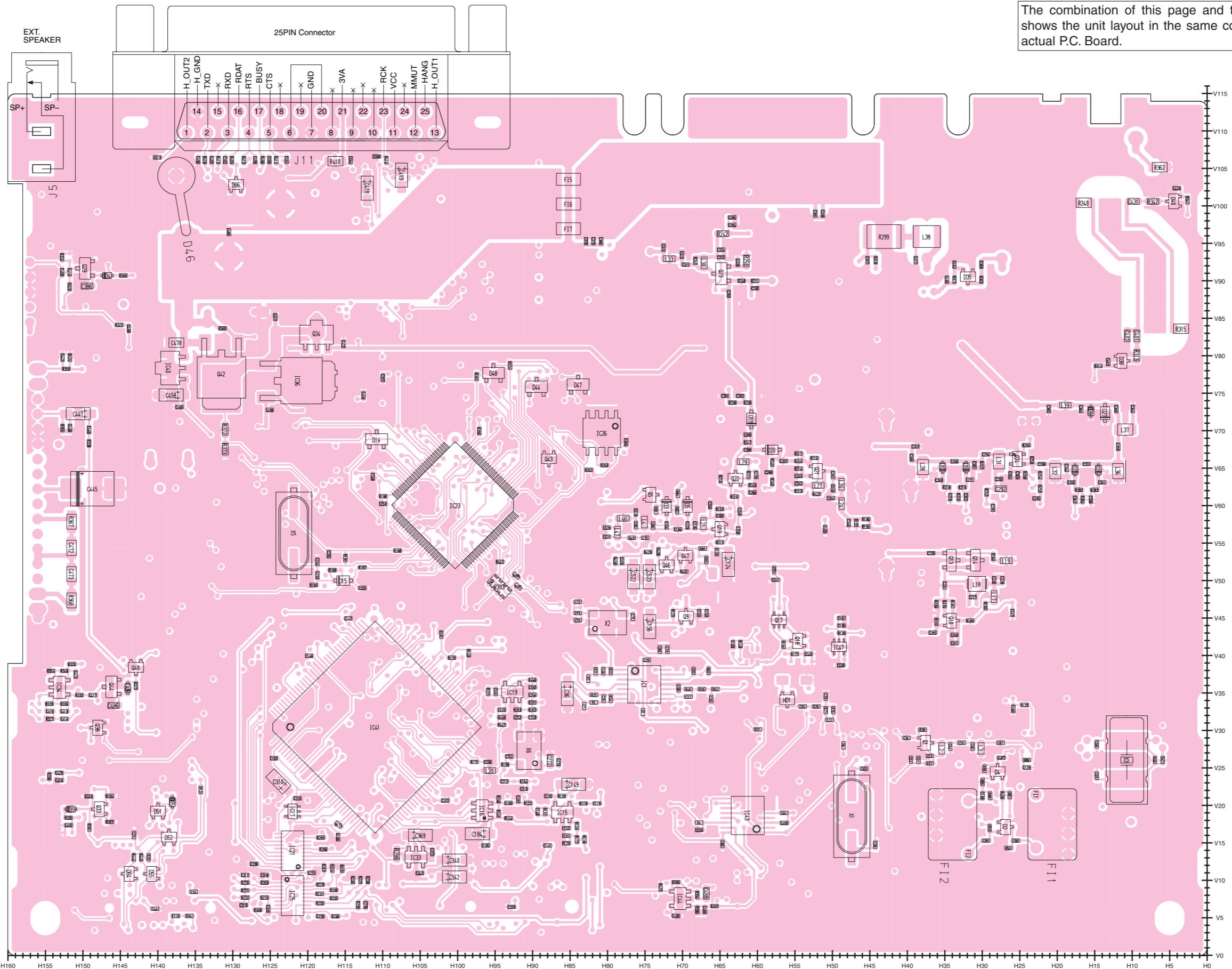
## 9-3 MAIN UNIT

### • TOP VIEW

The combination of this page and the next page shows the unit layout in the same configuration as the actual P.C. Board.

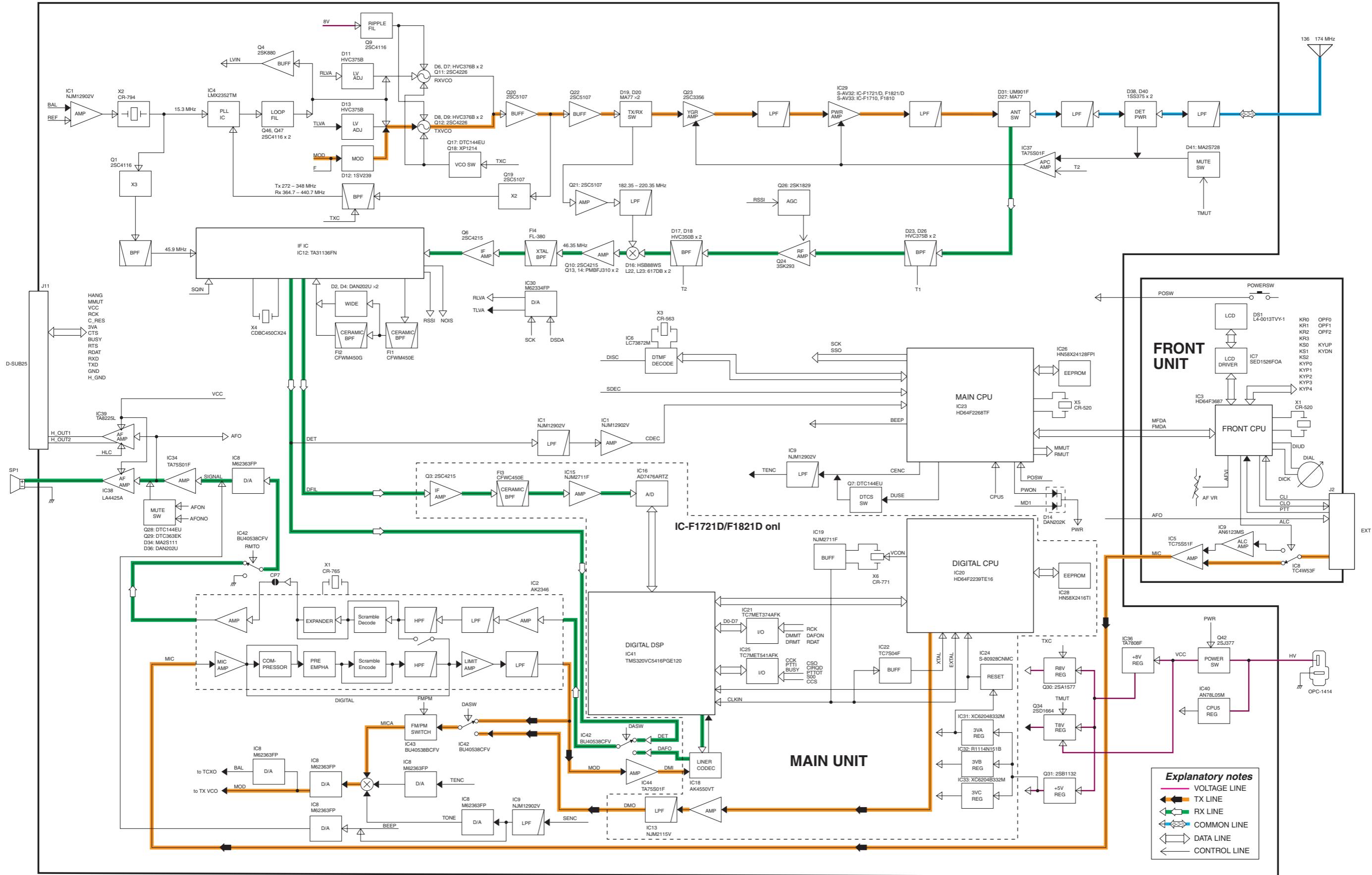


**MAIN UNIT**  
• BOTTOM VIEW



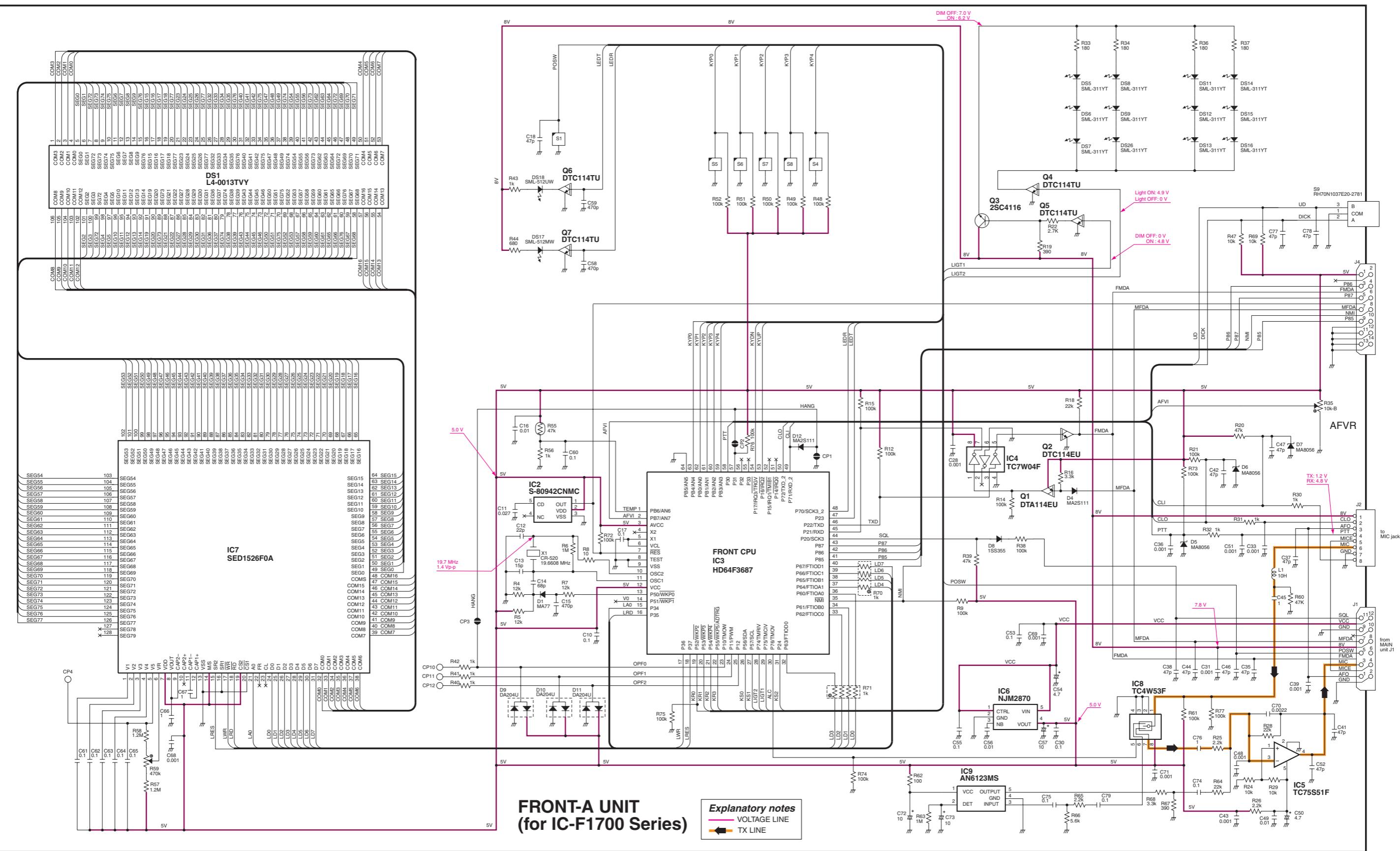
The combination of this page and the previous page shows the unit layout in the same configuration as the actual P.C. Board.

## SECTION 10 BLOCK DIAGRAM



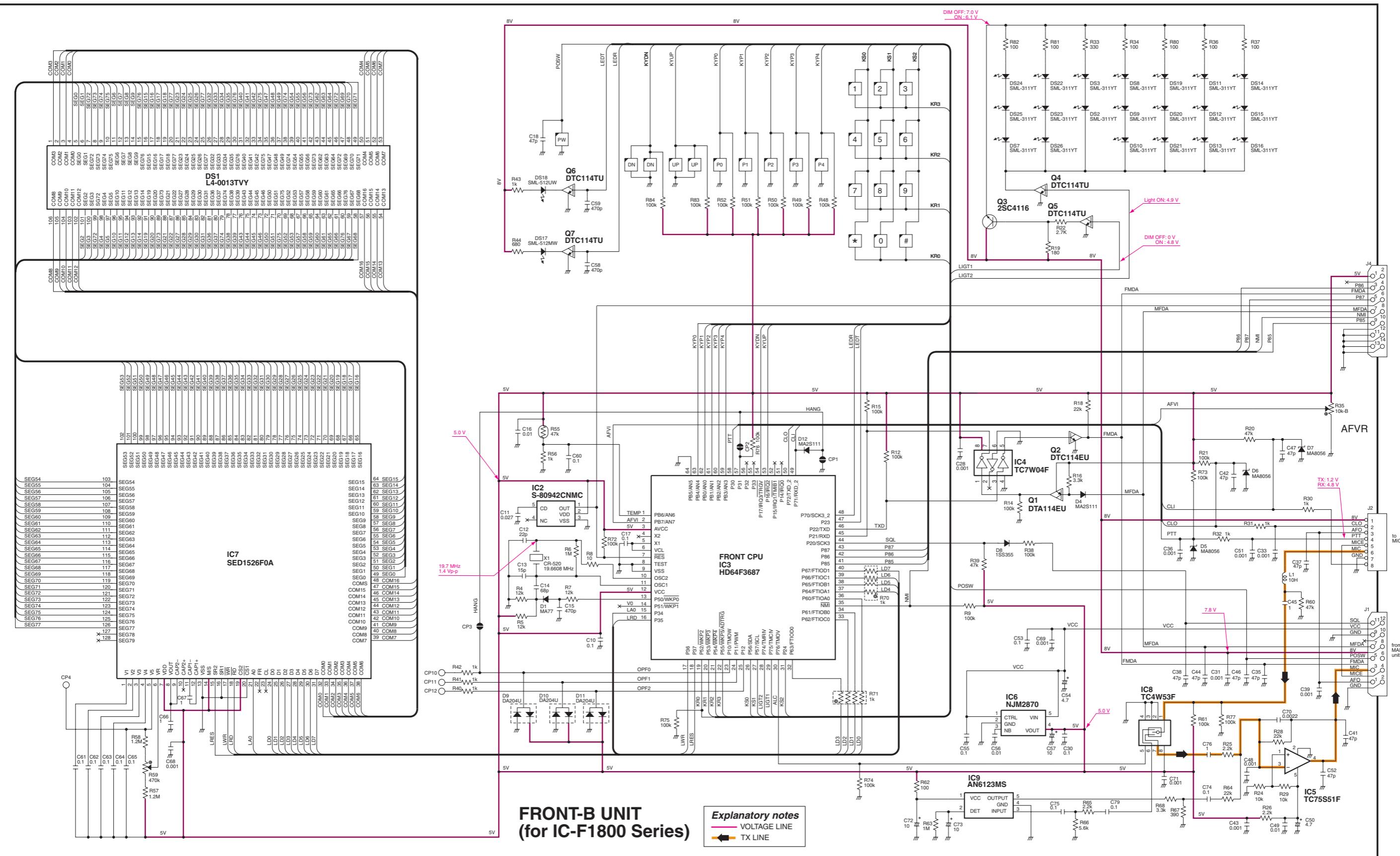
# SECTION 11 VOLTAGE DIAGRAM

## 11-1 FRONT-A UNIT (for IC-F1700 Series)

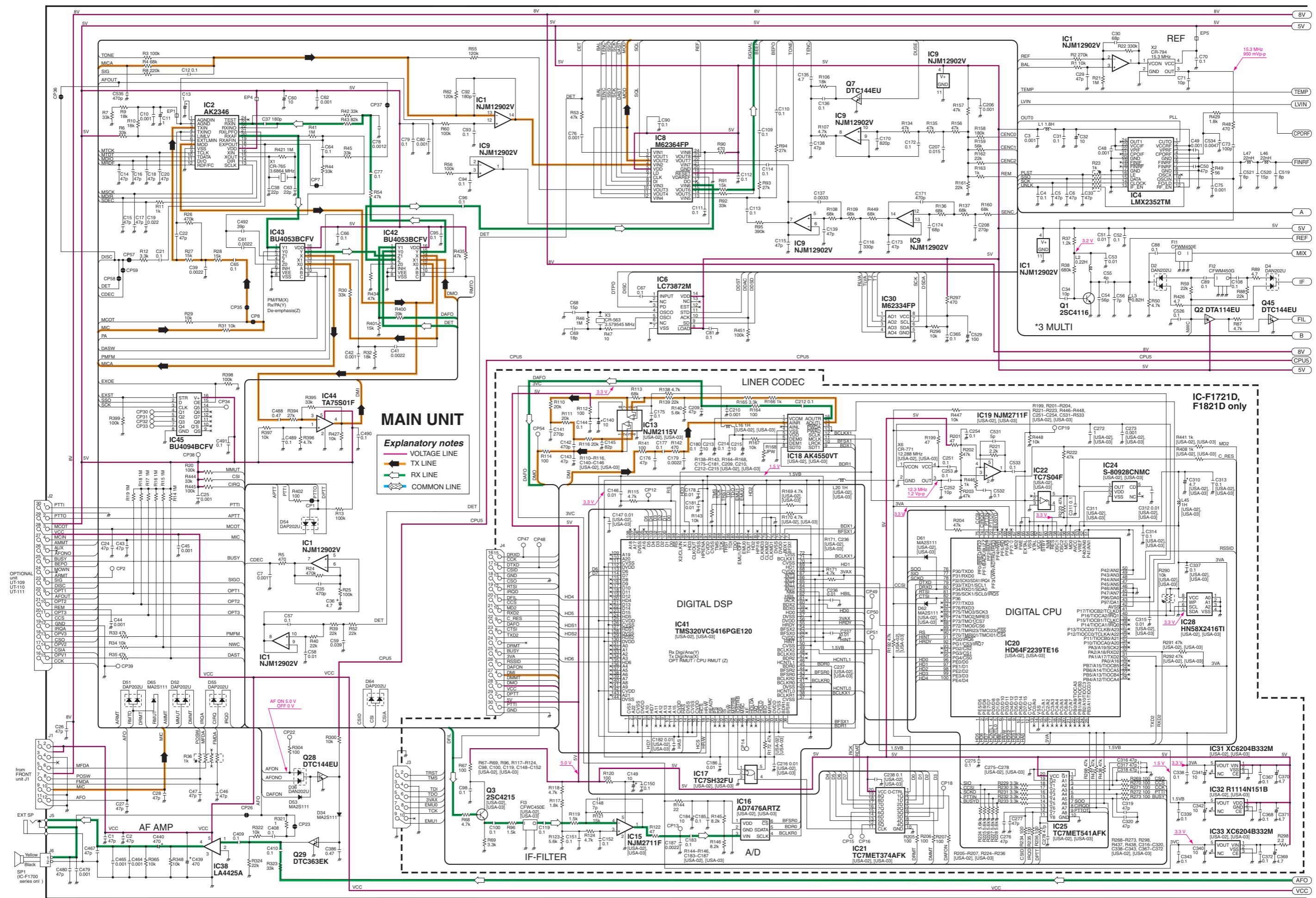


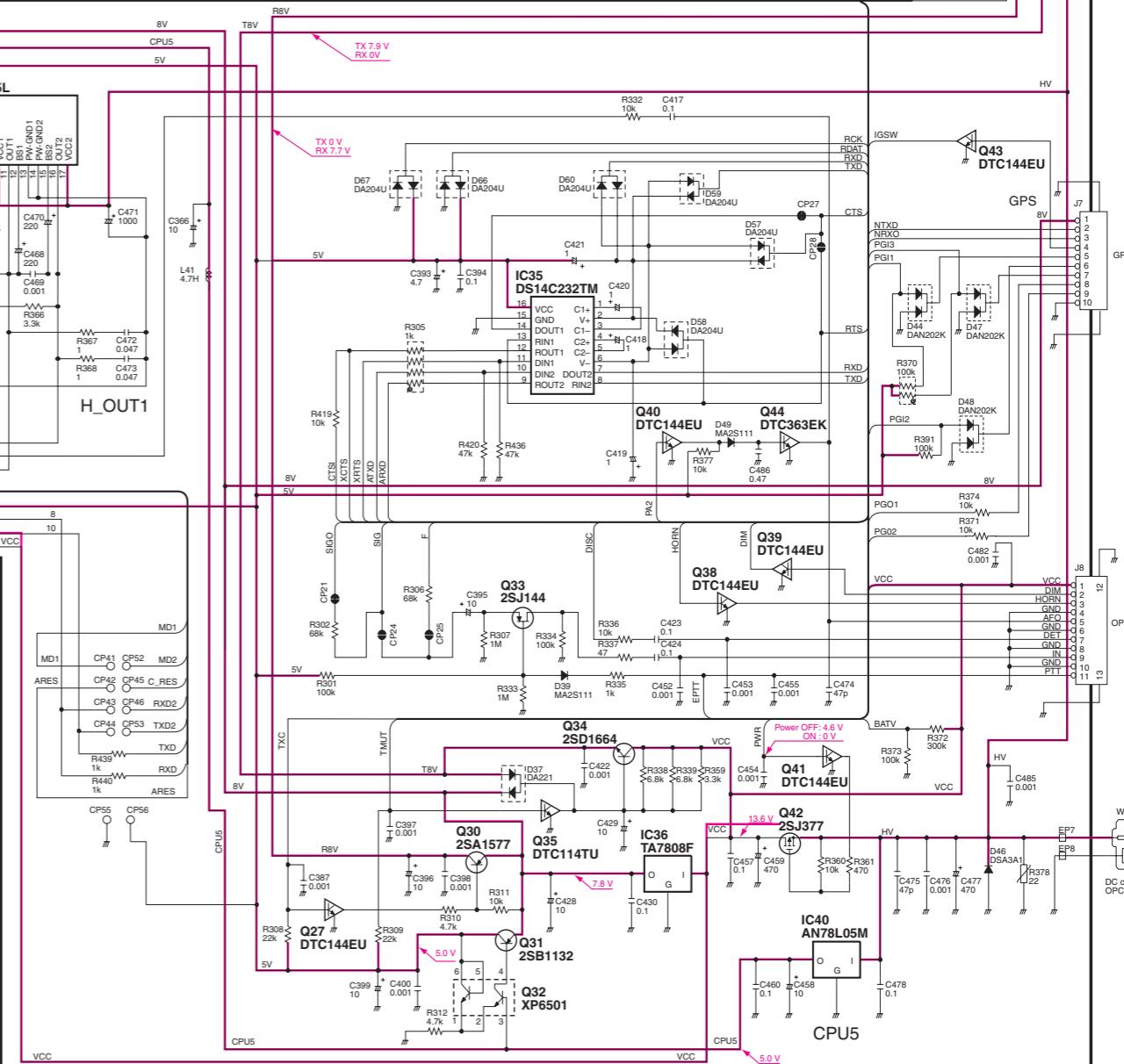
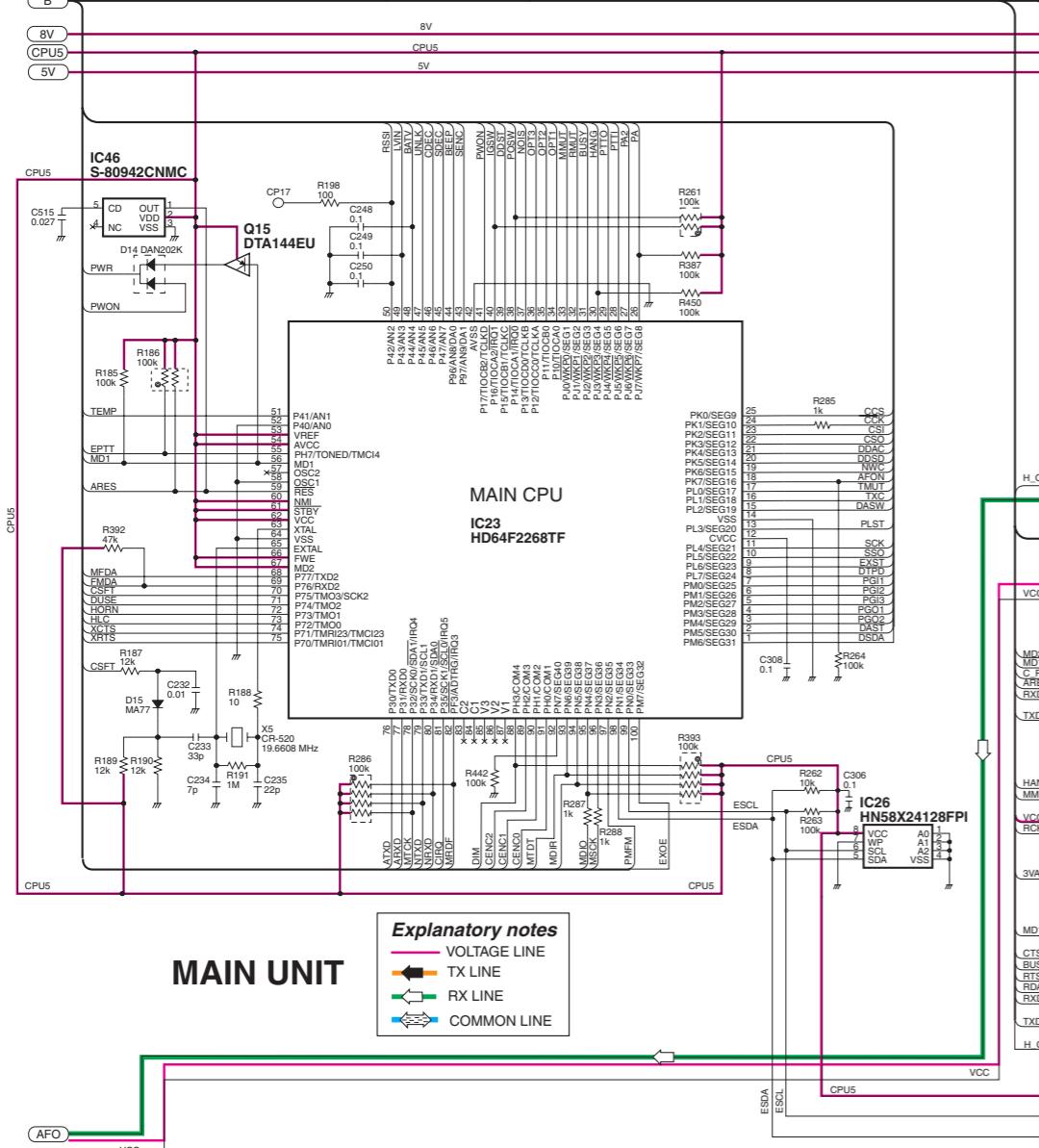
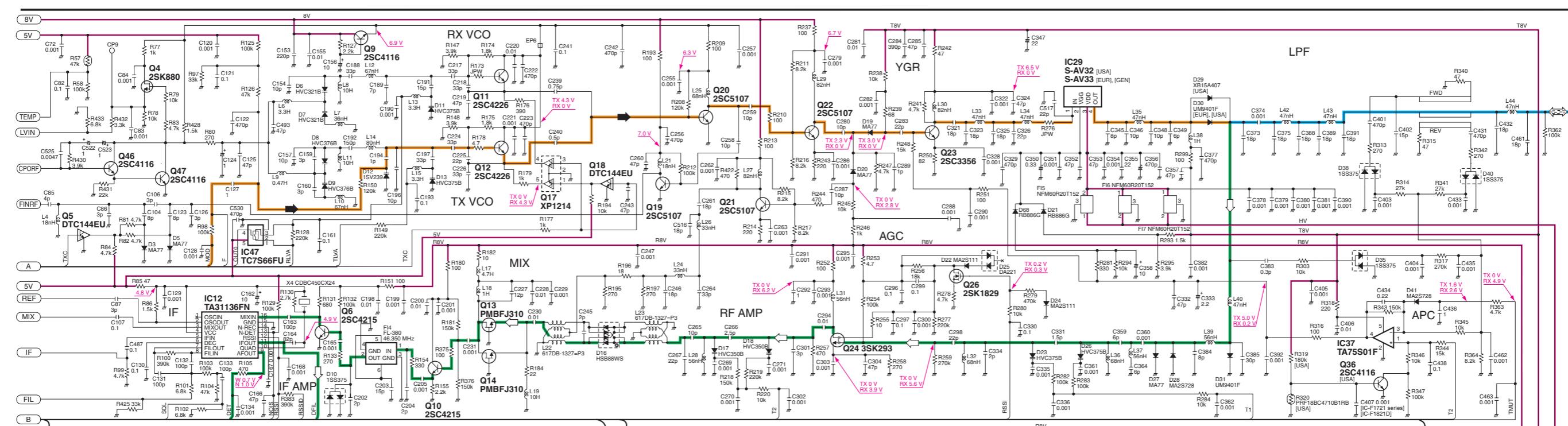
FRONT-A UNIT  
(for IC-F1700 Series)

## 11-2 FRONT-B UNIT (for IC-F1800 Series)



# 11-3 MAIN UNIT





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